

Monolithic front-end amplifier for portable laser rangefinder

Wang Zhuping, Liu Ruqing, Guo Xianju, Zhang Keshu

(Academy of Opto-Electronics, Chinese Academy of Sciences, Beijing 100094, China)

Abstract: A monolithic front-end amplifier for portable laser rangefinder was realized in 0.5 μm CMOS technology, owing to attaining adequate performance and lower cost simultaneity. It consists of transimpedance pre-amplifier (TIPA), differential voltage post-amplifier (DVPA), band gap reference and other interface circuits. Attention has been paid to design the TIPA and DVPA, which are most appropriate for the laser rangefinder signal processing. The measurement results show that the chip achieves 87.27 dB Ω transimpedance, 952.8 MHz bandwidth, 17.64 pA/Hz^{1/2} input referred noise current. The die area occupies 2.816 mm² including pads and dissipates 106.9 mW power consumption with 75% from the output buffer.

Key words: laser rangefinder; front-end amplifier; portable; regulated cascade; active inductance

CLC number: TN4 **Document code:** A **Article ID:** 1007-2276(2013)08-2050-05

应用于便携式激光雷达测距仪的单芯片全集成前置放大电路系统

王竹萍, 刘汝卿, 郭仙菊, 张珂殊

(中国科学院光电研究院, 北京 100094)

摘要: 基于 0.5 μm CMOS 工艺, 设计了一款应用于便携式激光雷达测距仪的单芯片全集成前置放大电路系统。该芯片主要由前置跨阻放大器(TIPA), 差分电压放大器(DVPA), 带隙基准源和其它接口电路构成。其中如何设计最适用于激光雷达测距信号处理系统的前置跨阻放大器和差分电压放大器是文中重点关注的对象。测试结果表明, 该芯片的跨阻增益可达 87.27 dB Ω , -3 dB 带宽 952.8 MHz, 输入等效参考噪声电流 17.64 pA/Hz^{1/2}。芯片面积为 2.816 mm²(包括焊盘面积), 功耗为 106.9 mW, 其中输出缓冲级功耗占 75%。

关键词: 激光雷达测距仪; 前置放大器; 便携式; 可调节共源共栅; 有源电感

收稿日期: 2012-12-30; 修订日期: 2013-01-31

基金项目: 国家高技术研究发展计划(2008AA121304); 国家科技支撑计划(2012BAH34801)

作者简介: 王竹萍(1983-), 女, 博士, 主要从事集成电路波行方面的研究。Email: wangzhuping169@163.com

0 Introduction

The goal of this work was to develop integrated signal processing circuit system for a portable laser rangefinder with a mm-level measurement accuracy. The operation of the pulsed time-of-flight (TOF) laser radar is based on the measurement of the transit time of a short laser pulse from the transmitter to the optically visible target and back to the receiver. It consists of a pulsed laser transmitter, transmitter and receiver optics, and receiver electronics. A high-precision and low-power front-end amplifier for receiver electronics has to be challenged to achieve the goal, which is the important part in the integrated signal processing circuit system and is to condition the received light current signal for analog voltage.

It is well known that the main factors limiting the measurement precision of a TOF laser radar are (1) bandwidth, which ensure the signal is processed without distortion, do not affect shape of the pulses and change their timing point, causing systematic errors; (2) noise, which causes random variation in the timing point and therefore limits the single-shot precision^[1]; (3) gain, which ensure echo signal is amplified to exceed the discrimination threshold and enlarge the measurement range of laser rangefinder. In addition, power consumption, size, cost, reliability also have to be considered in the design of front-end amplifier.

In this paper, the most recent work was reported. The monolithic front-end amplifier with high gain, appropriate bandwidth, low noise and cost will be introduced, which has been designed and implemented based on Central Semiconductor Manufacturing Corporation (CSMC) 0.5 μm double-poly three-metal (2P3M) 3.3 V CMOS technology, with satisfactory results. In order to set the scene for the reader, chip photomicrograph is shown in the third section of the paper. The whole chip including bonding pads occupies 2.816 mm². The pad size is minimal to achieve the lowest possible parasitic capacitance at the input node^[2].

1 Conceptual design

So the prospect to develop monolithic front-end amplifier is that, it has appropriate bandwidth, which has the lineal relationship with noise, owns enough gain, optimization noise, and offers lower-cost, power consumption and size.

One specific aim in this work was to improve the measurement precision by using high speed laser pulses. So the rise time of the signal is limited by the front-end amplifier, and the single-shot precision of the leading edge detection method can be shown as^[1]:

$$\sigma_R \approx \frac{0.35 \cdot c}{2 \cdot BW \cdot SNR} \quad (1)$$

Where c is the speed of light, SNR is the signal noise ration.

In practice, $SNR \geq 10$, so a bandwidth of 525 MHz is required to achieve a single-shot precision of 10 mm. Besides, the photodetector adopted in this work can export minimum light current of about 1 μA , and the discrimination threshold is mV-level usually. So the transimpedance gain should be at least 80 dB Ω .

2 Circuit design

The front-end amplifier described here and shown in Fig.1 is comprised by a transimpedance pre-amplifier (TIPA) with single-to-differential (STD) circuit, a differential voltage post-amplifier (DVPA) with output buffer (OB) (the output buffer is for test purposes only) and a band gap reference (it offers reference voltage and current to other functional blocks).

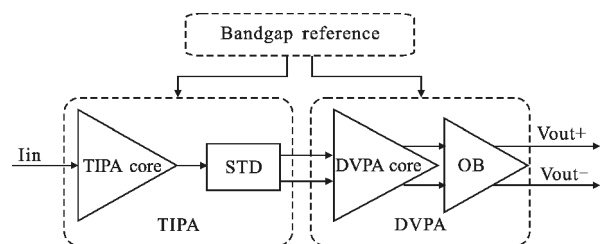


Fig.1 Proposed front-end amplifier framework

The incoming laser pulses are detected with a photodetector, which converts them to current pulses.

These current pulses are first converted to voltage pulses and amplified by the transimpedance pre-amplifier. Then the voltage pulses are further amplified to a level suitable by the DVPA, so that the voltage can be processed by the timing discriminator to produce accurately timed logic level pulses.

The TIPA shown in Fig.2 is composed of a current input stage, which is applied to alleviate bandwidth reduction of the TIPA due to large parasitic capacitance of the photodetector^[3], a core amplifier stage, feedback resistors and a single-to-differential circuit. Firstly, the single-ended structure was adopted in the TIPA to attain low-power and low-complexity. However, the DVPA was proposed in the post-amplifier, so a single-to-differential circuit has to be employed. Secondly, the regulated cascade (RGC) structure has also been applied in the input stage, because it could extend the bandwidth without a passive inductor, and thus the chip area can be saved well^[4-6].

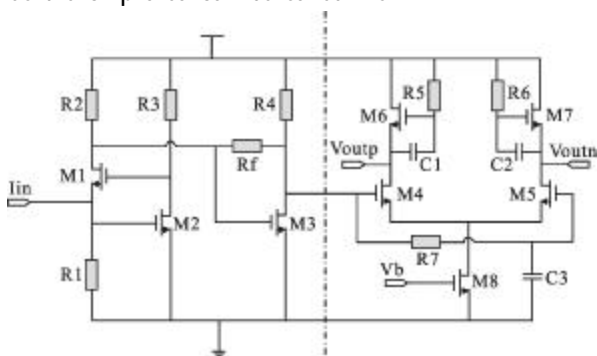


Fig.2 Transimpedance pre-amplifier with single to double circuit

In addition, noise optimization is processed.

Referring to the noise analysis in ref [7], neglecting the flicker noise, only considering the resistor and channel thermal noise, the equivalent input noise current spectral density of the TIPA is interrelated with $R1$, $R2$, Rf and $gm1$. To reduce the input noise current, the value of resistors and the size of transistors $M1$ should be increased as large as possible. But the change will result in bandwidth degeneration, so a choice of proper parameters and bias current is necessary to optimize the noise performance. The transimpedance of the TIPA is $4.2\text{ k}\Omega$.

As shown in Fig.3, the DVPA consists of cascaded gain stages to provide enough voltage gain, a wider bandwidth amplifier stage to further enhance the driver ability and an OB to drive the followed load for test^[8-9]. Firstly, it was implemented based on the differential architecture to improve the linearity, which in turn reduces the variation in the shape of the pulses, and therefore also their timing point, as a function of amplitude. Secondly, the active inductor technology was employed in the cascaded gain stages^[10]. So a wider bandwidth can be obtained though based on the conventional $0.5\text{ }\mu\text{m}$ CMOS process. Thirdly, the AC coupled inputs DC-offset isolation technology was adopted in the design that there is a small offset voltage between its inputs to increase the linear output voltage range. This can be done because the signal is a unipolar pulse with known polarity. The differential gain of the DVPA is 30 dB .

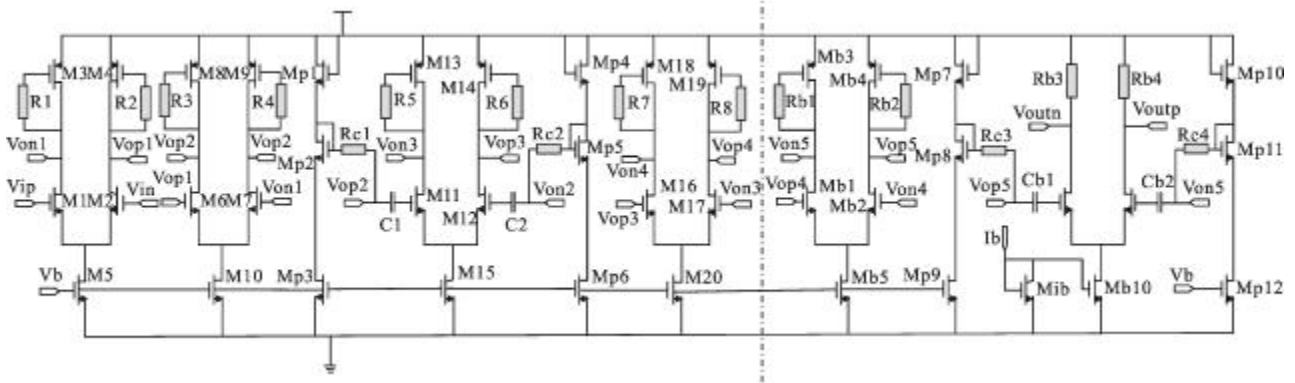


Fig.3 Differential voltage post-amplifier with output buffer

3 Measurement

Having finished the design and fabrication of the front-end amplifier (shown in Fig.4), the overall performance of the system was tested and verified in an Agilent open laboratory. Fig.5 shows the testing environment and apparatuses. The main characteristics of the amplifier measured are summarized in Tab.1.

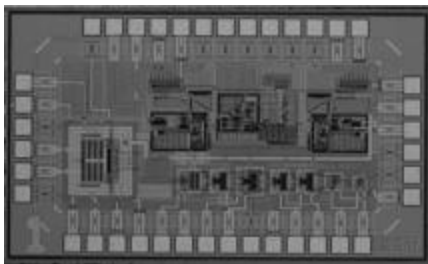


Fig.4 Front-end amplifier chip photomicrograph



Fig.5 Test environment and apparatus

Tab.1 Measured results summary

Supply voltage /V	Transimpedance /dBΩ	-3 dB Bandwidth /MHz	Input referred noise current density /pA·Hz ^{-1/2}	Power consumption /mW	Area /mm ²
3.3	87.27	952.8	17.64	106.9	2.816

The electrical performance of the amplifier was measured using the test printed circuit board (PCB) shown in Fig.6.

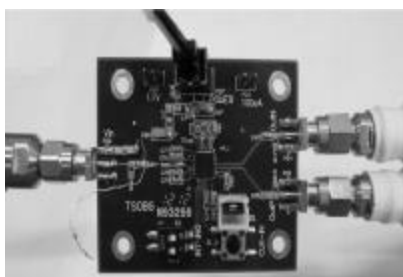
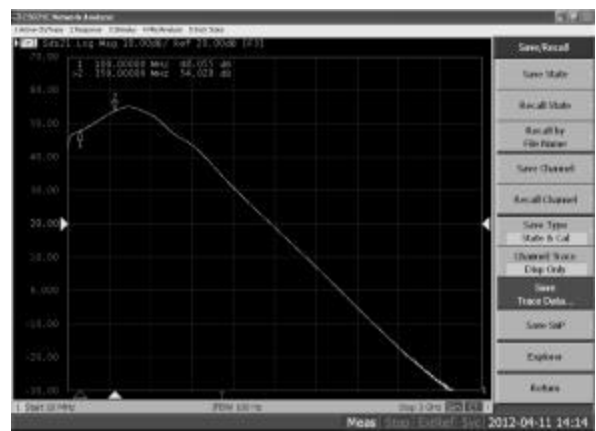
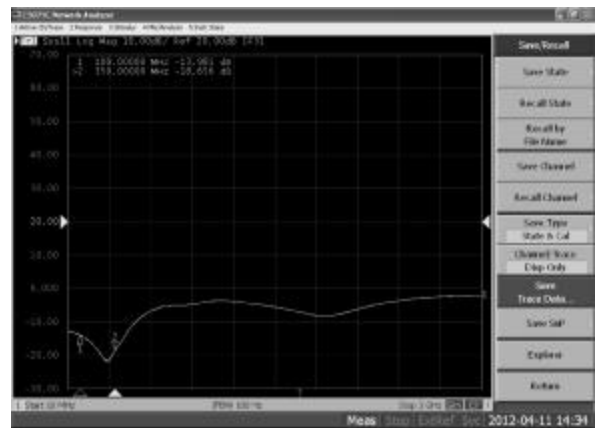


Fig.6 PCB test board

The transimpedance and bandwidth of the amplifier was measured by generating a single-ended current signal from a 50 Ω voltage output of a vector network analyzer (Agilent E5071C) with a resistive attenuator. Fig.7 shows the measured S -parameters (S21and S11) with an input signal power of -55 dBm. And the differential output transimpedance gain of amplitude-frequency response handling of equation(2). Fig.8 indicates that the differential output transimpedance gain is 87.27 dBΩ, -3 dB bandwidth of 952.8 MHz.



(a) S21 parameter



(b) S11 parameter

Fig.7 Measured S-parameters

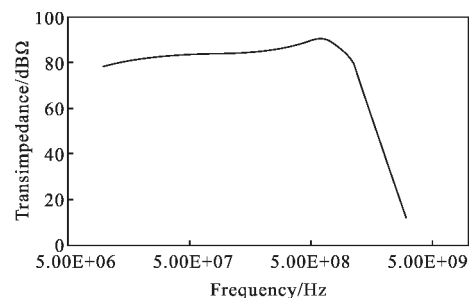


Fig.8 Measured amplitude-frequency response

$$|Z_{TIPA}| = \frac{|Z_0| \times |S_{21}|}{|1 - S_{11}|} \quad (2)$$

Generally, Z_0 is 50Ω .

The input-referred noise current density was measured by spectrum analyzer (Agilent N9020MAX), which owns the basic noise of $-160 \text{ dBm}^{[10]}$. Fig.9 shows the measured input-referred noise spectrum. The input referred noise current of front-end amplifier is $17.64 \text{ pA}/\text{Hz}^{12}$ at an input signal frequency of 350 MHz . They demonstrate a whole chip noise characteristic.

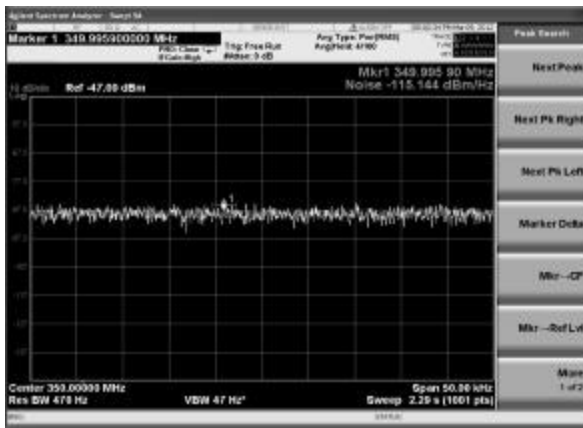


Fig.9 Measured noise spectrum

The output buffer, used only for testing purposes, attenuates the signal and increases its power consumption. The current consumption of the front-end amplifier is 106.9 mW from the 3.3 V supply. Thereinto, 75% is brought by output buffer.

4 Conclusion

This paper presents a front-end amplifier circuit applied in receiver electronics system for portable laser pulsed TOF rangefinder. Considering the special application of portable laser rangefinders, cost and power consumption, the monolithic circuit design method is chosen to implement the echo signal processing of laser radar. The hybrid circuit contains an analog circuit chip and a digital circuit chip. In this paper, the design of front-end amplifier chip has been presented, which is the basis to develop the whole integrated laser rangefinders signal processing

circuit system. And the functions have been verified through chip measurement, which agree well with the application requirement.

References:

- [1] Pennala R, Ruotsalainen I, Palojarvi P, et al. A 4 GHz differential transimpedance amplifier channel for a pulsed time-of-flight laser radar[J]. IEEE, 1998: 229-232.
- [2] Joyner V M, Zeng J. A CMOS imaging diversity receiver for gigabit free-space optical MIMO [J]. Analog Integr Circ Sig Process, 2011, 66: 371-379.
- [3] Chen W Z, Huang S H. A 2.5 Gbps CMOS fully integrated optical receiver with lateral PIN detector [C]//IEEE Custom Integrated Circuits Conference, 2007: 293.
- [4] Han S M, Sun G, Jiang F. Area-efficient CMOS transimpedance amplifier for optical receivers [J]. Analog Integr Circ Sig Process, 2009, 58: 67-70.
- [5] Bahram Zand, Khoman Phang, David A. A transimpedance amplifier with DC-Coupled differential photodiode current sensing for wireless optical communication[C]//IEEE, Custom Intergrated Circuits Conference, 2001.
- [6] J M Garc1'a del Pozo, W A Serdijn, A Ot1'n o S Celma. 2.5 Gb/s CMOS preamplifier for low-cost fiber-optic receivers [J]. Analog Integr Circ Sig Process, 2011, 66: 363-370.
- [7] Park S M, Yoo H J. 1.25-Gb/s regulated cascode CMOS transimpedance amplifier for gigabit ethernet applications[J]. IEEE J Solid-State Circuits, 2004, 39(1): 112.
- [8] Guo X J, Wang Z P, Zhang K S, et al. A low-cost, high-performance CMOS FDMA for optical communication systems [C]//The 8th International Conference on Wireless communications, Networking and Mobile Computing, Shanghai, 2012.
- [9] Huang H Y, Wen J C, Sun L L. 10 Gb/s CMOS limiting amplifier for optical transmission systems [C]//IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications Processings, 2005, 2: 859-862.
- [10] Liang B L, Kwasniewski T, Wang Z G, et al. A monolithic 10-Gb/s CMOS limiting amplifier for low cost optical communication systems[C]//APCC2008, 2008: 1-4.