340 GHz frequency multiplier without matching circuit based on Schottky diodes

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Abstract: Terahertz technology is a new across research field. In the last twenty years, THz technology has a great development. The multiplier was the very important aspect of the technology of terahertz heterodyne receiver front-ends in astrophysics, planetary and atmospheric sciences. THz gap exist in the application due to the lack of effective THz signal sources and detectors. Through the frequency multiple and amplification, we can get a high stability, low phase noise THz multiplier sources. 340 GHz is one of terahertz atmospheric windows, so 340 GHz multiplier source can be used in variety systems including communication and imaging system. The planar schottky diode based multiplier could work at room or low temperature. Multiplier was the most important part in terahertz multiplier chain. In this article, we have designed a 0.34 THz multiplier combined analysis of electromagnetic field theory and three-dimensional electromagnetic simulation software HFSS and ADS. The experimental results show that the max output is about 4.8 dBm, the max efficiency was 3%, in 331-354.5 GHz, and the output power was above 0 dBm. The results proved the correctness of the diode model and simulation.

Key words: THz technology; frequency multiple; simulation modeling; multiplication efficiency; Schottky diode; balanced multiplier

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340 GHz 基于肖特基二极管未匹配电路倍频源

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摘 要: 太赫兹技术是一个新兴的交叉研究领域。在过去 20 年,太赫兹技术有了巨大的发展。倍频器是太赫兹差分接收机重要技术,主要运用在天文、大气和行星科学射频前端。太赫兹空白的存在主要因素是缺少高效太赫兹源和探测器。通过倍频器技术和放大技术,可以得到高稳定低相噪的倍频源。340 GHz 是太赫兹大气传输窗口之一,所以 340 GHz 倍频源能够运用在各种通信成像系统中。肖特基二极管倍频源可以工作在常温和低温下。倍频器是倍频链路最关键的部分。通过理论分析和 3D 电磁仿真设计了一个 340 GHz 倍频器。实验得到最大输出功率为 4.8 dBm,最大效率为 3%,在 331~354.5 GHz

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输出功率大于 0 dBm。实验结果证明电路仿真和建模的可行性。

关键词：太赫兹技术； 倍频； 仿真模型； 倍频效率； 倍频源； 肖特基二极管； 平衡倍频器

0 Introduction

With the arrival of the information age, there is a demand for a large quantity of frequency multiplier chains for terahertz and sub-millimeter wave radar imaging system and space-based and ground-based terahertz wave super heterodyne receivers. There are several competing and demonstrating technologies in the semiconductor frequency multiplier field. Due to the internal symmetry, the Heterostruc-ture barrier varactors(HBV) usually produce only odd harmonics and some trippers were introduced in Ref.[1-3]. In Ref.[4] the quintuplers can reach its best conversion efficiencies to 5% at 210 GHz. Another important technology is about Planar Schottky diodes which were introduced in the late 1 990 s. Because of low output power of semiconductor three ports device, GaAs planar Schottky diode technology plays a crucial role in THz and sub-THz regions in two decades. Multiplier sources based on Schottky diode were characteristics of small volume, light weight, high reliability, and tunable broadband. At the same time, Schottky diodes were providing the best performance of efficiency and output power.

Frequency multipliers based on Schottky diode are nonlinear devices that generate harmonics of an input sine signal. Through a matching network at the input and output frequencies, we can optimize the transfer of power from the fundamental frequency to the desired harmonic and get the wanted harmonic and suppress undesired ones, Figure 1 shows the schematic diagram of the multiplier. Typically the order of multiplication of Schottky diodes is up to 3 and HBVs can be higher.

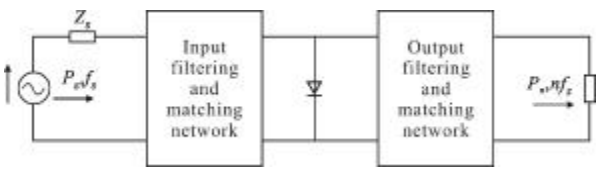

Fig.1 Schottky diode multiplier schematic diagram

Because the balanced multiplier has a high output power and efficiency, the balanced doubler becomes the popularity topology for frequency multiplication, proposed and tested in[4-7]. Some frequency multipliers have been shown in[8-10]. Doublers or triplers are the most important role at THz frequencies only, and demonstrated with reported powers at room temperature of 100 μW at 1.2 THz, 15-20 μW at 1.5-1.6 THz and 3 μW at 1.9 THz. In 2011, the article[11] report a 2.7 THz low power Terahertz multiplier source. The 2.7 THz multiplier chain included three Triplers, and the three balanced Triplers fabricate 5-μm-thin GaAs membrane and planar GaAs Schottky diode. The first stage had a 400 mW driver power at 100 GHz, and the output power was 35 ±3 mW at 300 GHz. The second stage adopted two ways Triplers combining based on power synthesis technology, got 1.3 mW at 828-918 GHz. At the final Tripler, we could get 2-14 μW at 2.49-2.76 THz. Due to the limit of planar Schottky Diode and membrane technics in China, most of multiplier had a low frequency and output power: the frequency is less than 200 GHz, the max output power up to 8 mW.

1 Theory of multiplier

The doubler refers to the Schottky diode non-linear characteristics (I-V or C-V characteristics) which can double the input single. Non-linear current-voltage and charge-voltage characteristics of a single diode can be expanded into power series on the excitation signal voltage **V**, the Eq.(1), (2) and (3):

$$\mathbf{V}=\mathbf{V}_s\cos\omega_s t \tag{1}$$

$$\mathbf{I}=\mathbf{a}_0+\mathbf{a}_1\mathbf{V}+\mathbf{a}_2\mathbf{V}^2+\mathbf{a}_3\mathbf{V}^3+\cdots\cdots \tag{2}$$

$$\mathbf{Q}=\mathbf{b}_0+\mathbf{b}_1\mathbf{V}+\mathbf{b}_2\mathbf{V}^2+\mathbf{b}_3\mathbf{V}^3+\cdots\cdots \tag{3}$$

Here, $\mathbf{a}_0, \mathbf{a}_1, \mathbf{a}_2, \mathbf{a}_3$ and $\mathbf{b}_0, \mathbf{b}_1, \mathbf{b}_2, \mathbf{b}_3$ are real constants, $\mathbf{V}_s$ is the input signal voltage. The number of diodes and the structure of circuit can affect harmonics' weight in Eq.(2) and (3).

Even frequency multiplication principle, if the input and output circuits made two diodes have a relation of Anti-Series, i_1, i_2, i_L, i would follow Eq.(4) in Fig.2.

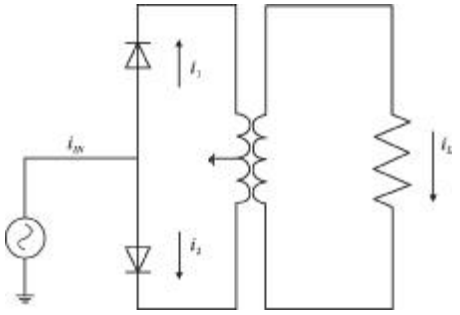

Fig.2 Equivalent circuit of Anti-Series diodes

$$\begin{cases} i=i_1(\mathbf{V})+i_2(\mathbf{V})=i_s(e^{\alpha V}-1)-i_s(e^{-\alpha V}-1) \\ i_L=i_1(\mathbf{V})-i_2(\mathbf{V})=i_s(e^{\alpha V}-1)+i_s(e^{-\alpha V}-1) \end{cases} \tag{4}$$

Here, α is a constant about temperature $\mathbf{T}$, i_s is the reverse saturation current, $\mathbf{V}$ is the signal voltage in Eq.(1). Simplify the Eq.(4) and get Eq.(5) which has shown the electric circuit is only suitable for even frequency multiplication. If the used diodes make the electric circuit appears unbalanced, the electric circuit function would grow worse, could not reach high efficiency.

$$\begin{cases} i=4i_s[I_1(\alpha\mathbf{V}_s)\cos\omega_s t+I_3(\alpha\mathbf{V}_s)\cos 3\omega_s t+\cdots] \\ i_L=i_s(2I_0(\alpha\mathbf{V}_s)-2)+4i_s[I_2(\alpha\mathbf{V}_s)\cos 2\omega_s t+I_4(\alpha\mathbf{V}_s)\cos 4\omega_s t+\cdots] \end{cases} \tag{5}$$

Here, I_0, I_1, I_2, I_3, I_4 were the constant coefficients, i was the input signal and i_L was the output current.

2 Design topology

In Terahertz Millimeter-wave band, the Schottky diode frequency multiplier had two basal design topologies: hybrid integration of discrete Schottky diodes[12] and non-substrate transmission line technique[13]. The later one requires higher technical demands of complete semiconductor process line and mainly applies to the frequency doubler higher than 600 GHz. Therefore, the 340 GHz multiplier used the hybrid topology which has been shown in Fig.3. The doubler efficiency has a clear correlation between the impedance in the input and output port of varactor and DC bias which is applied to the diode by using a microstrip diplexer. Allowing four anodes per chip has an advantage of dramatically increasing power handling capabilities and consequently the output power in Fig.3.

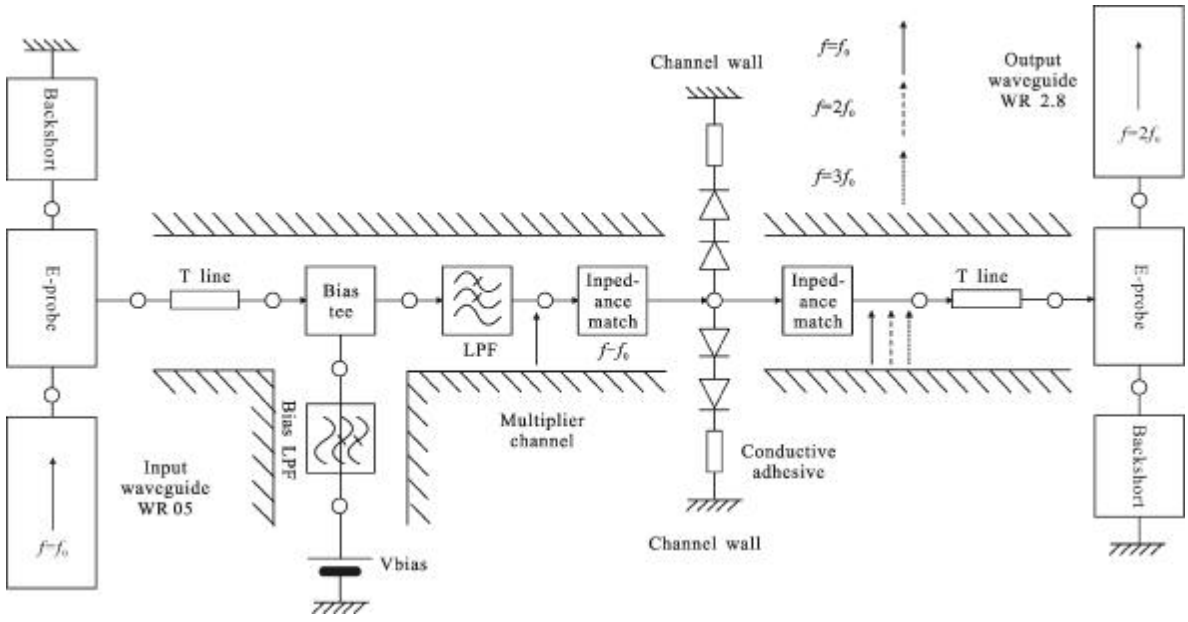

Fig.3 Block diagram of 340 GHz balanced doubler

The multipliers block diagram each consist of two components: nonlinear solid state devices (GaAs Anti-Series Air-Bridged Schottky Diodes or GaAs Anti-Parallel Air-Bridged Schottky Diodes) and the surrounding input, output waveguide and impedance matching microstrip circuitry.

3 Simulation of multiplier

This section will present a practical methodology that was used to design a wide-band frequency doubler at 340 GHz, and a number of important detailed points must be addressed.

3-Dimensional Modeling of the Schottky Diode in HFSS: accurately modeling the performance of the planar Schottky diode in the terahertz is a very delicate task. In order to avoid the influence of parasitical parameter, it's necessary to use the three-dimensional (3D) topology of the diode physics structure which features a variety of materials ranging from metals with low conductivity (ohmic contact) to highly doped semiconductors (N++ layer). Figure 4 has shown the 3D structure of the Schottky diode in 3D-electromagnetic field solver and every layer have been given the right material in HFSS shown in Tab.1.

Tab.1 Material of every layer in Schottky diode

Layers	Material
N	GaAs
Semi insulating	GaAs
Anode	Gold
Finger and pad	Gold
N+ and N++	PEC
Ohmic	PEC

In order to simulate the electro-magnetic behavior of the Schottky diode without junctions, a classical approach has been used in 3D-electromagnetic software using a wave port at the exact location of the Schottky contact. This wave port shown at red region in Figure 4 (a) is usually a small section of coaxial waveguide. The outer conductor of coaxial waveguide is buried in the N++ doped layer below the anode and inner conductor is connected to the anode and airbridge. The N++ doped layer is assimilated to a metal and it terminates the wave port on one side.

Figure 4(b), put the 3D diode model onto the quartz microstrip in waveguide channel, outgoing electromagnetic waves are generated, so input waves are received at output port, and S-parameters can be calculated in HFSS.

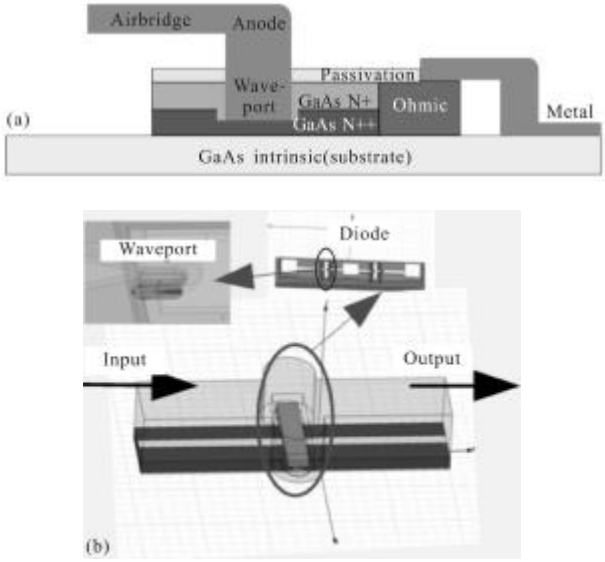

Fig.4 3D structure of Schottky diode model

Nonlinear Modeling of the Schottky Diode in ADS: Usually, the first step in the design of a frequency multiplier is to choose the diodes whose characteristics are the best suitable for the application. It includes doping density, the anode areas, junction capacitance $\mathbf{C}_j$, and breakdown voltage, the number of junctions, ideality factor η and 3D-electromagnetic model. The junction capacitance $\mathbf{C}_j$ and series resistance Rs are the most important parameters. For varactor Schottky diodes, the junction capacitance $\mathbf{C}_j$ is classically expressed as follow Eq.(6):

For $\mathbf{V} \leqslant \mathbf{V}_j/2$:

$$\mathbf{C}_j(\mathbf{V}) = \frac{\mathbf{A}\varepsilon_s}{t(\mathbf{V})} \quad \text{where} \quad t(\mathbf{V}) = \sqrt{\frac{2\varepsilon_s}{\mathbf{qN}_d}(\mathbf{V}_j - \mathbf{V})} \qquad (6)$$

For $\mathbf{V} \geqslant \mathbf{V}_j/2$, $\mathbf{C}_j(\mathbf{V})$ is defined by linear extrapolation of Equation (6) from $\mathbf{V} \leqslant \mathbf{V}_j/2$. Here **A** is the junction

area, $t(V)$ shows the thickness of the depletion layer, q shows the charge of the electron, N_d shows the doping of the semiconductor epilayer. The datasheet of the Schottky diode will normally give the value of N_d, C_j, A, V_j.

For the frequency multiplier with working at room temperature and $N_d=1\times10^{17}\,cm^{-3}$, the $C_j(0)$ and R_s meet Eq.(7).

$$R_s\times C_j(0)=120\Omega\times fF \tag{7}$$

This paper selected Schottky varactor diodes to design the 340 GHz multiplier. The diode has four single-pipe and Anti-Series structure. According to the parameters given by the datasheet, ideality factor η and series resistance R_s can be calculated, Figure 5 shows the model of single tube with the value of parameters.

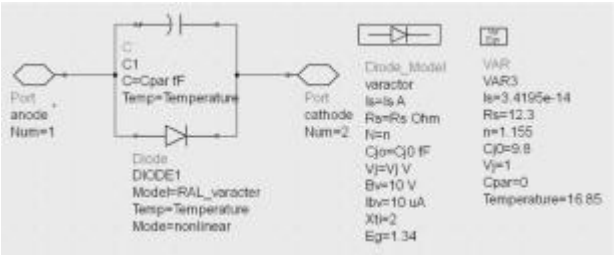

Fig.5 Model of single tube in ADS

Combine simulation methodology: In order to prove the correctness of the diode model and simulation, the input impedance is 70 Ω and the output impedance is 50 Ω. The structure of the multiplier uses 50 μm quartz microstrip circuit integrated in waveguide cavity. Figure 3 show that the doubler mainly includes five parts: input E-probe, varactor diode cave, input signal filter, DC bias and input E-probe. Figure 6 shows the three-dimensional (3D) structure model of the doubler in HFSS.

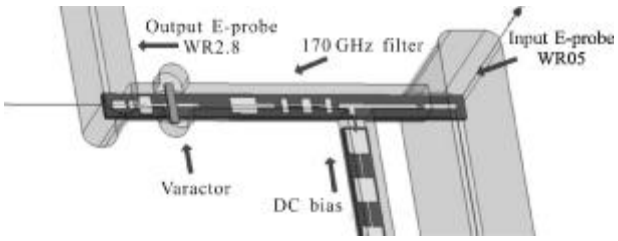

Fig.6 Three-dimensional structure model of doubler in HFSS

In order to get the efficiency of simulation for multiplier, the data with the SNP files format obtained from HFSS simulation are imported into ADS harmonic balance analysis circuit.

During the optimization, the bias voltage and the impedance of input and output port have a great influence to the efficiency of the doubler. The higher negative voltage will make the narrower the bandwidth and unmatched impedance will have a greater impact on efficiency and center frequency. For validating the accuracy of the model and developing the high bandwidth frequency doubler, 0 V bias voltage and 70 Ω input and 50 Ω output impedance are adopted. The relation curve of the frequency doubling efficiency and 20 dBm input power at 160-180 GHz is shown Fig.7.

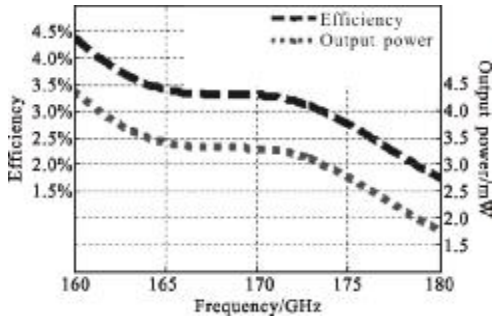

Fig.7 Simulation efficiency and output power of frequency doubler

4 Measurements and results

For the measurements, a commercial signal generator was used to driver an amplifier with max output power of 2 W at 39.5-45. Then through the two multipliers driver chain, a max output power 156 mW signal was got at 160-180 GHz, and this signal was used to driver 340 GHz doubler. For the room-temperature measurements, a calibrated WR10-WR2.8 was used to connect tested multiplier and PM power detector. Figure 8 has shown the measurements chain and the multiplier structure.

The measured results of 340 GHz multiplier is shown at room temperature in Figure 9. The measured results include four caves: Figure 9 (a) shows the

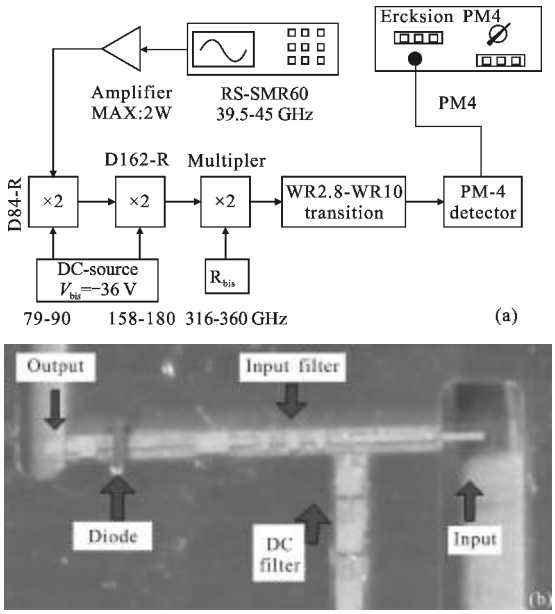

Fig.8 Measurements chain and structure of multiplier

efficiency in experiment and simulation and Fig.9 (b) shows the output and input power in experiment. The input power was 100-160 mW from 165.5-166 GHz and 167-177 GHz. The measured output power was 1 mW in the band 320.5-321 GHz, 332-334.5 GHz and 336.5-356 GHz, the low driver power caused the

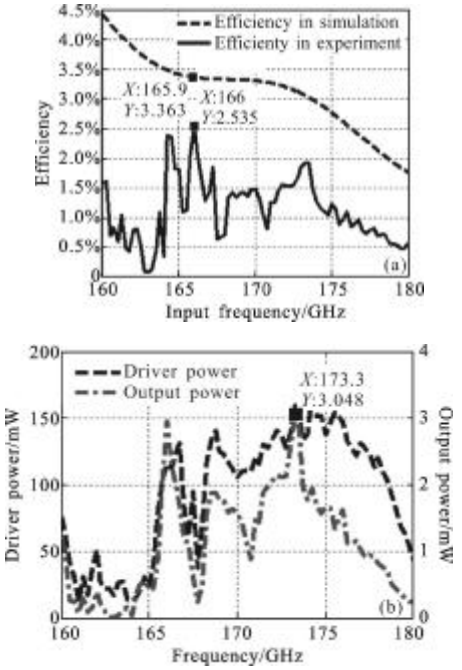

Fig.9 Results of 340 GHz multiplier in simulation and experiment

low output power in 321-332 GHz and 334.5-336.5 GHz. Fig.9 (a) shows the max efficiency of experiment is 2.54%, and the simulation efficiency is 3.36% at the same frequency point. In order to prove the output spectrum is local at 340 GHz, the 340 GHz receiver and 340 GHz band pass filter were used.

5 Conclusion

In recent years, there were tremendous progress in the modeling and fabrication of the frequency doubler at THz wavelengths for using simulation tools like HFSS and ADS. This multiplier with its driver forms a 340 GHz 2×2×2 multiplier chain, and the max output power is about 3 mW. Efficiency of experiment have the similar trend with simulation test curve: mutilation efficiency is higher at around of 165 GHz, at intermediate bandwidth changes gently and the higher frequency is lower. The successful design of 340 GHz multiplier shows the simulation modeling and fabrication can be applied to the THz wavelengths, the next work is using this method to design a high efficiency doublers with matching.

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