Design of CCD data acquisition system of miniature spectrometer

Zhang Ning, Liu Yulong, Wu Jiahui, Xu Xiping

(School of Opto-Electronics Engineering, Changchun University of Science and Technology, Changchun 130022, China)

Abstract: Miniature spectrometer is one of the main research directions in recent years. For the design requirements of the miniature spectrometer data acquisition system, the high-resolution data acquisition system was designed using TCD1304DG linear CCD. The system used FPGA EP4CE15 as the controlling core, the Analog Front End (AFE) chip as the main chip of the signal processing. The AFE chip integrated Programmable Gain Amplifier (PGA) and 16 -bit analog-digital convertor. High-speed data transmission circuit with USB2.0, the PC software of the spectral acquisition were designed, which realized the real-time processing of spectral data. The designed scheme of miniature integrated circuit meets the characteristics and requirements of the spectrometer of miniaturized and is portable to be used. Key words: miniature spectrometer; CCD; data acquisition; FPGA; USB2.0

CLC number: TN274.2; TP744.1 Document code: A Article ID: 1007-2276(2015)01-0141-07

微型光谱仪的 CCD 数据采集系统设计

张 宁,刘宇龙,吴嘉辉,徐熙平

(长春理工大学 光电工程学院,吉林 长春 130022)

摘 要: 微型光谱仪是近年来光谱仪发展的主要方向。针对微型光谱仪数据采集系统的设计需求,应用 TCD1304DG 线阵 CCD 完成了以 FPGA(EP4CE15)为控制核心的高分辨率数据采集系统设计,系统使用了集成 Programmable Gain Amplifier(PGA)、16 位模数转换功能的 Analog Front End(AFE)芯片, 开发了 USB2.0 高速数据传输电路并完成了光谱采集上位机软件的设计,实现了对光谱数据的实时 处理。小型集成的电路设计方案满足了光谱仪对小型化、便携使用的特点和要求。 关键词: 微型光谱仪; CCD; 数据采集; FPGA; USB2.0

收稿日期:2014-05-05; 修订日期:2014-06-03

作者简介:张宁(1979-),女,讲师,博士,要从事光电检测技术及质量控制有关方面的研究。Email:custzn@126.com

基金项目: 吉林省科技发展基金(20120357)

0 Introduction

Spect rometer is a kind of physical optical instrument, it uses the phenomena of dispersion, absorption and scattering to get the spectral related to substances, and realizes the analysis and measurement of the material's composition and structure [1]. Conventional spectrometer is complex, bulky, and slow in measurement speed. In order to meet the needs of real-time online testing, miniature spectrometer has become an inevitable trend in the development of spectrometer^[2]. To achieve the miniaturization of the spectrometer design mainly due to spectrographic structure optimization, the optical part using optical fiber transmission, asymmetric cross type Czernystructure and holographic grating, Turner optical electronics part uses the CCD array detection and high speed data acquisition system, the detector collects the effect light instantly after light splitting, which greatly acquisition improves the spectral speed, then, combines with computer technology, to achieve realtime spectral data output, and completes intelligent controlling and data processing of the spectrometer.

According to the characteristics of miniature spectrometer, CCD data acquisition system must has the function of data acquisition and processing, at the same time, it is also needed to satisfy the requirements of wide spectral range, compact structure, and low power. The parameters of the system are as follows: measuring spectral range is 380 - 780 nm; the measurement resolution is 1 nm; the data transmission speed is 200 frame/s; the volume of data acquisition part is not more than 1 000 cm³; the supplying power voltage is 5 VDC. The hardware system adopts TCD1304DG line array CCD, with 16 -bit AD converter for the acquisition of the CCD output analog signal, high-speed USB2.0 interface to transfer data, FPGA as the main control chip for the implementation of the CCD driver control, ADC conversion control, and USB transmission control. The software part is realized by VC++. The hardware part has the advantages of compact structure, low power consumption. The functions of spectral analysis software is flexible, has the characteristic of simple operation, and meets the need of high speed and high resolution on-line detection.

1 Basic structure of miniature spectrometer

The structure diagram of miniature spectrometer is shown in Fig.1. The system uses optical fiber as

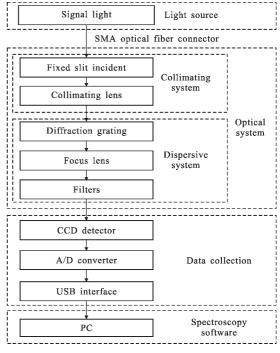


Fig.1 Structure diagram of miniature spectrometer

the signal coupling device, the light passes through the fixed slit into the grating splitting system, the optical systems with asymmetric cross Czerny-Turner structure achieve light collimating and dispersion. The light is received by the CCD detector after splitting, each of the CCD detector pixels responses the signals of different wavelengths, thus obtains the optical signal intensity corresponding to different wavelength. The analog optical signal output of the CCD device is converted to digital signal using AD converter, then the digital optical signal is sent to the upper computer through the USB data bus. Finally, the data is dealt with by the spectroscopy software to obtain the complete spectrum.

2 Data acquisition system

This section focuses on the design of data acquisition system, the system is mainly for TCD1304DG linear CCD used in miniature spectrometer. According to the data flow, the system is divided into three functional modules, that is: CCD timing and driver module, signal conditioning and AD module, data transmission and communication module. The structure diagram of spectral data acquisition system is shown in Fig.2.

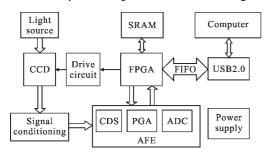


Fig.2 Structure diagram of spectral data acquisition system

This system uses EP4CE15^[3] as the main control chip, the FPGA not only provides the three-phases CCD drive signal timing and the ADC sampling reference timing, but also controls the USB interface chip and data transmission communication. CCD timing and drive module provide CCD driving pulse signal according to the requirements of CCD, and desired signal level through CCD driver chip. The signal conditioning circuit completes buffering, amplification, filtering and preprocessing to the analog signal of the CCD output, and the AFE chip AD9826 adjusts PGA appropriately and converts the analog signal to 16-bit digital signal. Data transmission and communication module puts the 16-bit of the CCD digital signal for storage, and transfers data to computer through the USB interface, the PC can also send commands via the interface to control CCD data to be acquisited. The USB port provides total power supply of the system directly, but due to different computer's USB output power and voltage fluctuations, the system uses a slight boost circuit to control 5 V

power supply, and then uses power chip LDO providing stabilized voltage required by each chip.

2.1 CCD timing and drive module

The spectral response range of TCD1304DG ^[4] linear CCD is between 200–1100 nm, the peak wavelength is 550 nm, which meets the requirement of measuring spectral range, TCD1304DG has 3 648 pixels, so the theory resolution of data acquisition system can reach 0.1 nm, the pixel size is $8 \mu m \times 200 \mu m$, large size image sensing element can guarantee high sensitivity. At the same time, the CCD has electronic shutter can adjust optical integral time according to the signal intensity flexibly. The output signal without reset level and does not require CDS, the power supply voltage is 5 V, suitable for USB direct power supply equipment.

Using the Modelsim, we simulate CCD driver control timing, and CCD driver timing and AD clock simulation are shown in Fig.3.

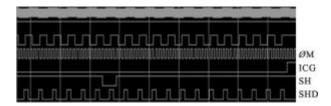


Fig.3 CCD drive timing and AD clock simulation

The system provides three pulse signals by the FPGA, these signals are SH transfer pulse signal, ICG light integral control pulse signal and ØM master clock signal. During the high level of SH signal, the signal charging of photosensitive area is transferred in parallel to the simulation shift register, and during the low level of SH signal, photosensitive area is isolated to analog shift register. Therefore, as shown in a drive row with multiple SH cycles, which can realize the adjustment of CCD exposure time. The ICG signal is equivalent to the enable signal of the device, it produces deep potential well in photosensitive area when ICG is high level, and light integral begins. Therefore the ØM signal after the rising edge of ICG is used as a starting point the CCD output data. In this system, using the 48 MHz clock as FPGA reference

clock, the rest of the clock are obtained by the clock frequency divider.

2.2 Signal conditioning and A/D module

Under the action of transfer pulse \emptyset M, the output of each CCD pixel corresponds to analog signal between 0 to 5 V, the signal is first sent to a pre-buffer amplifier and then to the A/D. Taking into account of the power supply of the system and the bandwidth of CCD output signal, it choses AD8032 with 5 V power supply as a preprocessing circuit amplifier, whose 80 MHz bandwidth and 30 V/ μ s slew rate meet the system requirements sufficiently. The circuit schematic of signal conditioning is shown in Fig.4.

By the 24 frequency division of FPGA reference

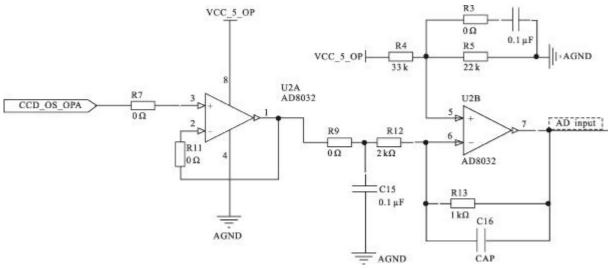


Fig.4 Circuit schematic of signal conditioning

clock 48 MHz, we get the 2 MHz frequency of CCD master clock ØM. The data rate of CCD is a quarter of the master clock, after another frequency division, and then FPGA sends this clock to SHD. To ensure the acquirement of the CCD output data stability and quickly, we must use high-speed A/D conversion device. The choice is AD9826^[5] high-speed CCD front-

loading signal processing AFE chips, it has a 16-bit AD resolution, the maximum permissible switching frequency is 15 MHz. With 1-6 times programmable amplifier, using a three-wire serial communication configuration related registers, AD9826 can configure CDS mode, gain, offset, and so on. The circuit schematic of 16-bit A/D is shown in Fig.5.

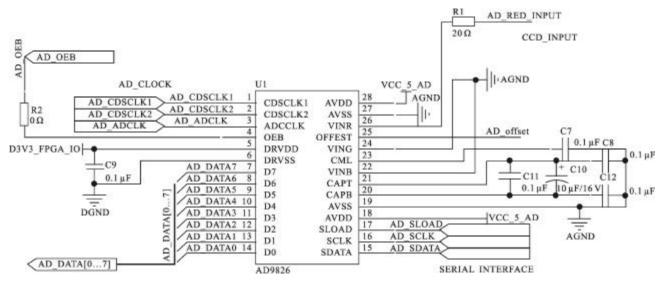


Fig.5 Circuit schematic of 16-bit A/D

This design uses single-channel mode, the acquisition mode set to SHA. Initialization does not use internal gain, so it should to configure AD9826 internal registers. When the system needs to change the CCD acquisition system working state, we can use upper computer to send commands to change the gain exposure time setting. There are two important parameters, one is CONFIGURATION:9' b011_001_000; another is MUXCONFIG:9'b011_000_000.

According to the output data pattern of AD9826 being mixed with high 8-bit and the low 8-bit, while in the FPGA program, data processing algorithms and communication are used with the 16-bit cache, so it requires 8 -bit to 16 -bit conversions for data by FPGA.

2.3 Data transmission and communication interface Under the design of USB2.0 high speed communication transmission, it uses Cypress' s CY7C68013A^[6] chip as USB2.0 interface chip in order to meet the system's transmission speed stability, development flexibility. CY7C68013A chip uses synchronous SlaveFIFO interface mode for spectroscopic data transmission. In SlaveFIFO mode, processor cannot interfere with data transmission, it only needs TD_Init() function to configure CY7C68013A working mode and the relative registers. USB controller endpoint is set to 512 bytes, the buffer depth is level 4, using the BULK mode to transfer, and has the automatic input mode.

In order to ensure high-speed communications, the working state of the system is divided into two steps, namely, data acquisition and data transmission. As the arrival of each AD clock, FPGA will get from AD a set of data stored synchronously in off-chip SRAM. It will be sent to upper computer, when data is transmitted.

According TCD1304DG datasheets, the maximum data rate of this kind CCD is 1 MHz, in case of not considering invalid pixel points, the approximate data amount of one frame is 3700 pixels, the data acquisition time should be $1 \times 3700 = 3700$, that is 3.7 ms, thus

the theoretical maximum frame rate is 270 frames/s. In this design, the effective data communication rate of USB2.0 is 25 MHz, since the controller endpoint is 512, the transmission data amount must be an integer multiple of 512, the amount of data designed is 4 609. Therefore, the theoretical time of every data transfer is $512 \times 9 \times 0.04 \ \mu s = 0.184 \ ms$. In other words, the communication rate of USB2.0 CCD acquisition rate is far less than the USB communication speed, most of the time, the system is working in the AD acquisition state.

3 Spectral analysis system software design

Based on Microsoft VC++, the driving program of USB2.0 and spectral data acquisition and processing software are developed. The flowchart of USB interface program is shown in Fig.6, at the beginning of the program, the first work is initialization, that is, open the USB device and download the firmware, then wait for the event occurs, when the event in progress, calls the dynamic link library function to send data command and the parameters, and finally close the device. The processed events of USB are mainly divided into two kinds of data transmission and parameter settings, The CCD parameters need to be configured when working are mainly gain, exposure time, etc.. The computer send the commands to FPGA via the USB interface.

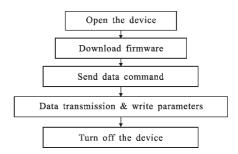


Fig.6 Flowchart of USB interface program

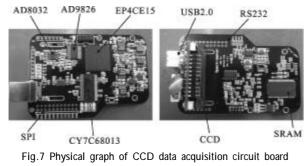
Spectral analysis software is composed by data source, spectral data display and data acquisition toolbar, the software can be a single frame or continuous data collection, it also can complete the integration time of the CCD and set the PGA gain basic parameter, where integration time can be disposed between 16 ms to 64 ms.

In order to ensure that the software is compatible with other CCD models and spectral device, software will number each device and after completing initialization, it will send device information to the computer, and then the data source list will show the basic parameters of the devices. Spectral data display module has two files which can be switched, including data tables and waveform curve chart. Data tables can show every pixel value, waveform curve chart contains a variety of visualization tools, which can set the display range, zoom window, etc. Under spectral wave curve chart displays the peak wavelength information. By setting the minimum peak width and base line, we can find out the peak which meets the conditions. Data collection toolbar has data averaging, smoothing, dark noise removal and other basic algorithm tool.

To facilitate system commissioning and secondary development, the underlying driver is made into dynamic link library by using VC++, then the upper application software can call the dynamic link library file to realize the corresponding functions.

4 Analysis and test results

The physical graph of CCD data acquisition circuit board is shown in Fig.7. The entire circuit board length is 8 cm, width is 6 cm, high is 4 cm, using USB port power supply, voltage is 5 V, the maximum current is 200 mA, and the actual power consumption is less than 1 W.



The spectroscopy software interface is shown in Fig.8, the spectrum shown is low pressure mercury lamp spectral data whose scanning speed is 200 frames/s, grating measurement is in the zero order light position, measuring peak wavelength of mercury lamp corresponding to pixel position is shown in Tab.1.

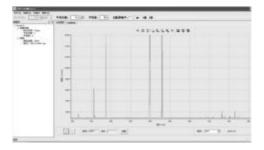


Fig.8 Spectroscopy software interface

Tab.1 Measuring peak wavelength of mercury lamp corresponding to pixel position

Wave- length /nm	365	405	408	436	546	577	579
Pixel	84	391	415	635	1 521	1 777	1 794

The experimental results show that, the system is stable and reliable, low noise, spectrum with good repeatability, integral time control accurately, complies with the requirements of spectrometer.

5 Conclusions

This paper studied the CCD data acquisition system of miniature spectrometer, designed the data acquisition system FPGA using as the core component, completed 16-bit data conversion through interface extension and data transmission based on USB2.0, achieved 200 frames/s rate. The system is flexible, portable and scalable, and is a better spectrometer data acquisition program for miniature spectrometer, which meets the requirements of realtime measurement of spectrometer.

References:

James J F, Sternberg R S. The Design of Optical Spectrometers
[M]. London: Chapman and Hall LTD, 1969: 20-80.

- [2] Jose Higino Correia, Marian Bartek, Reinoud F Wolffenbuttel. High selectivity single-chip spectrometer in silicon for operation at visible part of the spectrum [J]. IEEE Transactions on Electron Devices, 2000, 47(3): 553-559.
- [3] Altera. Altera Cyclone IV datasheet [R/OL].<u>http://www.altera</u>. com.cn/literature/lit-cyclone-iv.jsp. 2013.
- [4] Toshiba Semiconductor.TCD1304DG Datasheet[R/OL]. http://

www.dzsc.com/datasheet/TCD1304DG_1687764.html. 2012.

- [5] Analog Devices. Complete 16-bit Imaging Signal Processor AD9826 [R/OL]. <u>http://www.analog.com/en/prod/0,2877</u>, AD9826,00.html. 2007.
- USB Implementers Forum.Universal Serial Bus Revision 2.0 specification [R/OL]. <u>http://www.usb.org/developers/docs/</u>. 2012.