

## 70 nm gate-length InAs PHEMTs with maximum oscillation frequency of 640 GHz

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**Abstract:** Because of the high electron mobility and two-dimensional electron gas concentration, InP based pseudomorphic high electron mobility transistors (PHEMTs) become one of the most promising three-terminal devices which can operate in terahertz. The InAs composite channel was used to improve the operating frequency of the devices. The two-dimensional electron gas(2DEG) showed a mobility of  $13\ 000\ \text{cm}^2/(\text{V}\cdot\text{s})$  at room temperature. 70 nm gate-length InAs/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  InP-based PHEMTs were successfully fabricated with two fingers  $30\ \mu\text{m}$  total gate width and source-drain space of  $2\ \mu\text{m}$ . The T-shaped gate with a stem height of 210 nm was fabricated to minimize parasitic capacitance. The fabricated devices exhibited a maximum drain current density of  $1\ 440\ \text{mA}/\text{mm}$  ( $V_{\text{GS}}=0.4\ \text{V}$ ) and a maximum transconductance of  $2\ 230\ \text{mS}/\text{mm}$ . The current gain cutoff frequency  $f_T$  and the maximum oscillation frequency  $f_{\text{max}}$  were 280 and 640 GHz, respectively. These performances make the device well-suited for millimeter wave or terahertz wave applications.

**Key words:** InAs-channel; high electron mobility transistor; T shaped gate;  
maximum oscillation frequency

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## 最大振荡频率 640 GHz 的 70 nm 栅长 InAs PHEMTs 器件

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**摘要:** 由于高的电子迁移率和二维电子气浓度, InP 基赝配高电子迁移率晶体管(PHEMTs)器件成为制作太赫兹器件最有前途的三端器件之一。为提高器件的工作频率, 采用 InAs 复合沟道, 使得二维电子气的电子迁移率达到  $13\ 000\ \text{cm}^2/(\text{V}\cdot\text{s})$ 。成功研制出 70 nm 栅长的 InP 基赝配高电子迁移率晶体管, 器件采用双指, 总栅宽为  $30\ \mu\text{m}$ , 源漏间距为  $2\ \mu\text{m}$ 。为降低器件的寄生电容, 设计 T 型栅的栅根高度达到 210 nm。器件的最大漏端电流为  $1\ 440\ \text{mA}/\text{mm}$  ( $V_{\text{GS}}=0.4\ \text{V}$ ), 最大峰值跨导为  $2\ 230\ \text{mS}/\text{mm}$ 。截止频率  $f_T$  和最大振荡频率  $f_{\text{max}}$  分别为 280 GHz 和 640 GHz。这些性能显示该器件适于毫米波和太赫兹波应用。

**关键词:** InAs 沟道; 高电子迁移率晶体管; T 型栅; 最大振荡频率

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## 0 Introduction

For high resolution imaging and high-frequency wireless communication applications such as medicine, remote atmospheric sensing and radar systems, it is essential to fabricate a low-noise amplifier(LNA) with high gain, large bandwidth, and low power consumption<sup>[1-6]</sup>. InP -based pseudomorphic high electron mobility transistors(PHEMTs) have been proved to be the most promising devices for such demands, because of their high electron mobility, high saturation velocity, and high sheet electron density in the high indium content InGaAs channel <sup>[7]</sup>. The performances of PHEMTs become much better with the increase of indium content. Therefore, the InAs material shows great potential as a channel candidate in high-frequency PHEMTs. Recent reports of record high-frequency characteristics as assessed by the current-gain cutoff frequency  $f_T$  and the maximum oscillation frequency  $f_{max}$  of InAs PHEMTs, have been published. Current records for  $f_T$  and  $f_{max}$  are 644 GHz using a 30 nm gate-length technology <sup>[8]</sup> and 1.5 THz using a 25 nm gate-length technology<sup>[9]</sup>, respectively.

In this paper, the design, fabrication, and characteristics of 70 nm gate-length InAs PHEMTs were described. Source and drain ohmic contacts were formed with non-alloyed Ti/Pt/Au. The T-shaped gate with a stem height of 210 nm was fabricated to minimize parasitic capacitance. The frequency characteristics of  $f_T=280$  GHz,  $f_{max}=640$  GHz, and  $G_{m,max}=2\ 230$  mS/mm of the device were demonstrated.

## 1 Device fabrication

The epitaxial layers of the PHEMTs were grown on semi-insulating (100) InP substrate by metalorganic chemical vapor deposition (MOCVD). As shown in Fig.1, the layer structure consists of an  $In_{0.52}Al_{0.48}As$  buffer layer, a very thin channel that is composed of  $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ , an  $In_{0.52}Al_{0.48}As$  barrier, an InP etching stop layer, and a bulk-doped

$In_{0.53}Ga_{0.47}As$  cap layer. An Si doping plane was inserted in the Schottky layer to supply electrons for current conduction. The results of hall measurements on this structure with the cap layer removed showed a two-dimensional electron gas (2DEG) sheet density of  $3 \times 10^{12} \text{ cm}^{-2}$  and a mobility of  $13\ 000 \text{ cm}^2/(\text{V} \cdot \text{s})$  at room temperature.

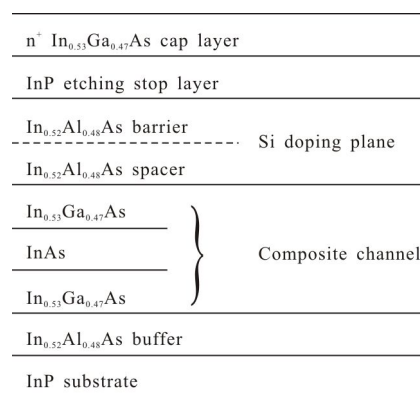


Fig.1 Schematic of the material structure of InAs PHEMTs

The process of device fabrication was simple. First, the mesa isolation was done by means of a phosphorus acid based wet chemical etching to expose the  $In_{0.52}Al_{0.48}As$  buffer layer. Then, source and drain ohmic contacts were formed with non-alloyed Ti/Pt/Au with a spacing of  $2 \mu\text{m}$ . Transmission line method (TLM) measurements revealed the contact resistance of  $0.067 \Omega \cdot \text{mm}$  on linear TLM patterns, which could be further reduced using improved process.

The T-shaped gate process was the most difficult due to its small gate length. A conventional tri-layer resist (ZEP/PMGI/ZEP) was used for EB lithography. After definition of the bottom ZEP layer, the top layers were exposed and developed, which eliminated the effect of gate head exposure energy into the bottom resist layer during gate foot development, so that a much smaller line could be achieved. A two-step recess process was then used to expose the InAlAs barrier. The T-shaped gate with a Ti/Pt/Au metal stack was fabricated with a stem height of 210 nm to minimize parasitic capacitance. Finally, the devices were fully passivated with plasma-enhanced chemical

vapor deposition  $\text{Si}_3\text{N}_4$ . SEM images of an InAs PHEMT and 70-nm T-shaped gate were shown in Fig.2.

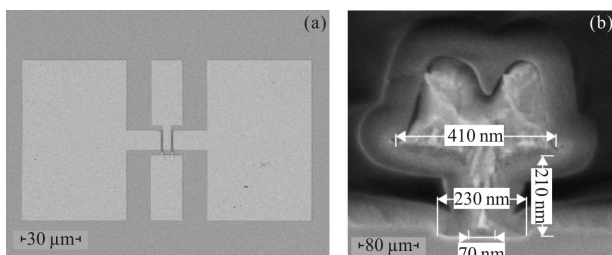


Fig.2 SEM images of (a) an InAs PHEMT and (b) 70-nm T-shaped gate

## 2 Results and discussion

The current-voltage characteristics of fabricated PHEMTs with two fingers 30  $\mu\text{m}$  total gate width measured at room temperature are shown in Fig.3. The gate-source voltage ( $V_{\text{GS}}$ ) is decreased from (top) 0.4 V to (bottom) -0.6 V in steps of -0.2 V. Good pinch-off characteristics were observed at  $V_{\text{GS}}=-0.6$  V. The drain-source current ( $I_{\text{DS}}$ ) reached about 1 440 mA/mm at  $V_{\text{DS}}=1.5$  V and  $V_{\text{GS}}=0.4$  V. The drain current rises with the increase of drain-source voltage ( $V_{\text{DS}}$ ) at  $V_{\text{DS}}>0.5$  V, which is attributed to impact ionization because of the narrow band-gap of InAs channel. Figure 4 shows the  $V_{\text{GS}}$  dependence on the  $I_{\text{DS}}$  and transconductance ( $G_m$ ) of the PHEMTs when biased at  $V_{\text{DS}}$  of 0.8 V. The device shows a threshold voltage ( $V_{\text{Th}}$ ) of about -0.35 V. An maximum transconductance ( $G_{m,\text{max}}$ ) of 2 230 mS/mm is obtained at  $V_{\text{GS}}=-0.24$  V, which is attributed to shorter gate-length and higher mobility of InAs channel material.

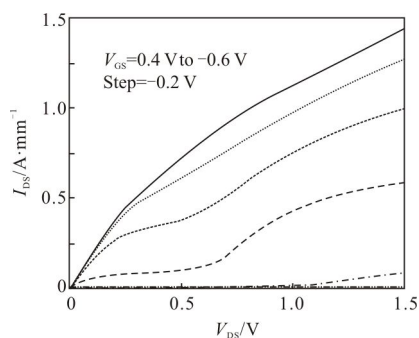


Fig.3 Output characteristics of the InAs PHEMTs

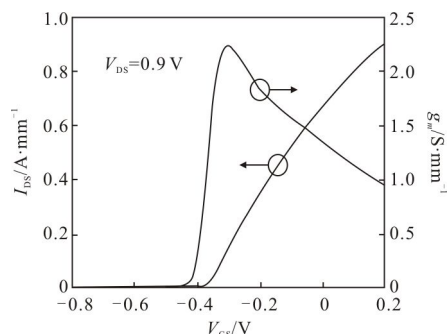


Fig.4 Transfer characteristics of the InAs PHEMTs

On-wafer small-signal RF performances of devices were characterized with a vector network analyzer, which swept from 1 to 110 GHz and 90 to 140 GHz. S-parameter measurements for open and short pads were also performed on the same wafer in order to calibrate the parasitic capacitance and inductance components related to the pad metals. The current gain  $H_{21}$  and the maximum stable gain/maximum available gain (MSG/MAG) of devices were derived from measured S-parameters as a function of frequency. The small signal characteristics of the device with a 70 nm gate length are shown in Fig.5. A cut-off frequency  $f_T$  of 280 GHz was obtained by extrapolating  $H_{21}$ , and a maximum oscillation frequency  $f_{\text{max}}$  of 640 GHz was achieved by extrapolating MAG/MSG using a least-square fitting with a -20 dB/decade slope.

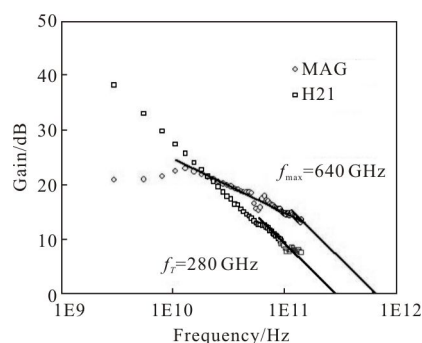


Fig.5 Small signal characteristics of the InAs PHEMTs

Figure 6 shows  $f_{\text{max}}$  as a function of  $L_g$  for sub-100 nm InGaAs and InAs PHEMTs. When the gate-length is smaller than 50 nm, the short channel effect becomes more severe and the effect of parasitic

parameters becomes bigger. So it is difficult to improve the frequency performance by simply reducing the gate-length of the device. Due to the decrease of parasitic capacitance, the obtained  $f_{max}$  value in our devices is higher than most of ever reported in PHEMTs above  $L_g=70$  nm. The excellent frequency performances promise the possibility of THz –wave applications, especially for W –band millimeter-wave devices and circuits. More outstanding device performances would be obtained by optimizing the material structure, reducing the gate length of T–gate and the space of drain-to-source.

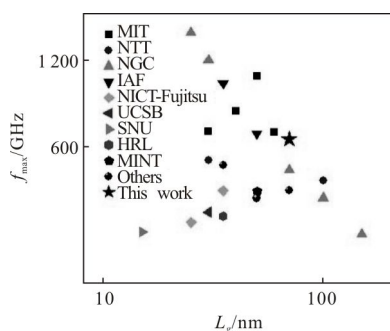


Fig.6  $f_{max}$  as a function of  $L_g$  for reported InGaAs and InAs PHEMTs in the literature<sup>[8-27]</sup>

### 3 Conclusion

In summary, 70 nm gate-length InP–based InAs PHEMTs have been fabricated. A T–shaped gate with a stem height of 210 nm was used to minimize parasitic capacitance. The maximum drain current density and maximum peak transconductance were 1 440mA/mm and 2230mS/mm, respectively. Meanwhile, a current gain cut-off frequency of 280 GHz and a maximum oscillation frequency of 640 GHz were obtained. The excellent performance can be attributed to the high mobility of the InAs material and the short gate-length. Further device fabricated technology can be used to improve device DC and RF performances, such as reducing the source-drain space, gate-length and so on.

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