12-bit compact multiple-columns-shared-parallel pipeline-SAR ADC for high speed CIS

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Abstract: A multiple-columns-shared-parallel pipelined successive approximation register (SAR) analog-to-digital converters (ADC) was presented for high speed CMOS image sensors (CIS) application. As the pixels in 8 columns shared one pipeline-SAR ADC, the layout was no longer restricted to double pixel pitches, and can be implemented within 16 pixel pitches. Asynchronous logic was implemented to improve the conversion speed of multiple-columns-shared-parallel pipeline-SAR ADC. A half-gain multiplying digital-to-analog converter (MDAC) was used for the residue amplification to relax the requirements for the operational amplifier (opamp), and correlated level shift technique was also used for more precise amplification. The 12-bit resolution was divided by 6-bit coarse and 7-bit fine SAR sub-ADC with 1-bit stage redundancy calibration between coarse and fine steps. Input full scale voltage was 1 V. The ADC was designed in 0.18 μm 1P4M CIS process, and occupied 0.204 mm^2 for 8 columns. The simulated results of the ADC showed a SNDR of 72.6 dB with a 229.7 kHz input and 71.7 dB with a 4.16 MHz input at 8.33 Msps. It dissipated 4.95 mW at 1.8 V supply and the FoM was 172.5 fJ/conversion-step. Because the pixel pitch is only 7.5 μm and the process has only 4 metals, this proposed 12-bit multiple-columns-shared-parallel pipeline-SAR ADC is quite suitable for the high speed CIS.

Key words: high speed CIS; multiple-columns-shared-parallel; pipeline-SAR ADC

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用于高速 CIS 的12-bit 紧凑型多列共享并行 pipeline-SAR ADC

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摘 要:设计了一款用于高速 CMOS 图像传感器的多列共享列并行流水线逐次逼近模数转换器。八列像素

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共享一路 pipeline-SAR ADC,从而使得 ADC 的版图不再局限于二列像素的宽度,可以在 16 列像素宽度内实现。该模数转换器采用了异步控制逻辑电路来提高转换速度。半增益数模混合单元电路被用于对第一级子 ADC 的余差信号放大,同时被用于降低对增益数模混合单元电路中运放性能的要求。相关电平位移技术也被用于对余差信号进行更精确的放大。整个 pipeline-SAR ADC 第一级子 ADC 精度为 6-bit,第二级子 ADC 为 7-bit,两级之间存在 1-bit 冗余校准,最终实现 12-bit 精度。输入信号满幅电压为 1 V。该 8列共享并行处理的 pipeline-SAR ADC 在 0.18 μm 1P4M 工艺下制造实现,芯片面积为 0.204 mm^2。仿真结果显示,在采样频率为 8.33 Msps,输入信号频率为 229.7 kHz 时,该 ADC 的信噪失真比为 72.6 dB;在采样频率为 8.33 Msps,输入信号频率为 4.16 MHz 时,该 ADC 的信噪失真比为 71.7 dB。该 pipeline-SAR ADC 的电源电压为 1.8 V,功耗为 4.95 mW,功耗品质因子(FoM)为 172.5 fJ/conversion-step。由于像素尺寸只有 7.5 μm,工艺只有四层金属,因此这款 12-bit 多列共享列并行流水线逐次逼近模数转换器非常适用于高速 CMOS 图像传感器系统。

关键词:高速 CMOS 图像传感器; 多列共享列并行; pipeline-SAR AD

0 Introduction

High speed CMOS image sensor (CIS) and infrared image sensor are widely used in various fields such as motion analysis, machine vision and scientific research [1-2]. It consists of two critical components: high-speed high-sensitivity pixels, fast and accurate readout circuits. In fact, a high-speed high-resolution ADC is one of the most critical building blocks in the readout chain. It is also a huge challenge to design an ADC with small area and low power for the high speed CIS. In consideration of the area, power, resolution and speed requirements, column-parallel ADC has been proven to be an effective architecture[3-4]. For column-parallel architecture, each column is equipped with a readout circuit, which is placed in the space of double pixel pitches. The ADC array is usually distributed in both sides of the pixel array. Recently, high speed CIS also calls for high resolution more than 1 920×1 080 for some applications[5]. The high speed high resolution CIS has a large focal plane and produces a more strict constraint on the area of the ADC. Thus, it is essential to decrease the pixel pitch and improve the speed of the readout circuit, so that several columns of pixel′s output signals can be processed by a shared ADC [6-7]. Multiple-columns-shared architecture is effective to reduce the number of ADCs and the readout circuit area. The ADC layout is no longer confined to a very narrow space.

Several ADCs for high speed CIS have been reported. The single-slope ADC is a compact and simple architecture, but its conversion rate is seriously limited by the clock frequency. The cyclic ADC is another simple architecture for image sensors. It uses one stage elements to convert all bits by passing its residue back to its own input. As it only digitizes 1.5-bit each step and thus it takes several steps to finish the quantization. As a result, the cyclic ADC has a limited conversion speed[8]. The SAR ADC has been a very popular architecture for image sensors. It only consists of a comparator, a binary capacitor DAC (CDAC) and a feedback logic. The weaknesses of SAR ADC are speed limitation and complex capacitor array with complicated routing for high resolution. Due to the above drawbacks, it becomes more and more difficult to implement a high resolution high speed SAR ADC in single column pitch less than 15 μm[9-10]. The SAR ADC is simple and can achieve a moderate speed and resolution. The pipeline ADC can achieve higher

speed and the sub-stage ADC is easy to be shared. Sampling rates, resolution and power efficiency of the pipeline ADC can be increased by using a SAR ADC as the sub-ADC[11].

This paper proposes a multiple-columns-shared-parallel pipeline SAR ADC for high speed CIS. A 260×130 pixel array with 7.5 μm pitch 4T pixel and the proposed circuits are designed in 0.18 μm 1P4M CIS process and implemented on a 3.8 mm×4.9 mm die. As the pixel pitch is very small and the process has only 4 metals, multiple-columns-shared pipeline-SAR ADC is suitable for this design. The ADC is implemented within 16 pixel pitches. Asynchronous logic is implemented to improve the conversion speed of the SAR sub-ADC and control the MDAC automatically. A half-gain MDAC architecture with correlated level shift technique is used for the precise residue amplification and relaxing the requirements on the opamp. Metal-insulator-metal (MIM) capacitor and electrical field shielding MOM capacitor are used as the unit capacitor of the first stage and second stage SAR sub-ADC, respectively. Dynamic comparator is used to quantify the input difference signal. 1-bit stage redundancy is applied to resolves the 12-bit resolution after digital error correction. The following sections make a detail description about the design of the proposed multiple-columns-shared-parallel pipeline-SAR ADC.

1 Architecture

Figure 1 shows the pixel array and the preprocess module for the CIS, the pixel array signals are readout row by row. The analog preprocess circuits convert the single-ended pixel signal to difference signal and amplify the pixel signal. The ADCs perform quantization operations for the preprocessed pixel signal.

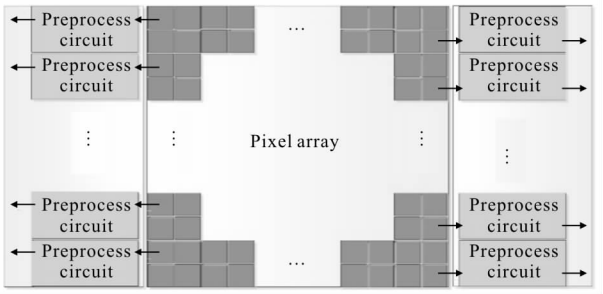

Fig.1 Pixel array and the preprocess circuit

The architecture of the proposed 12-bit compact multiple-columns-shared-parallel pipeline-SAR ADC for the high speed CIS is shown in Fig.2. It consists of several main building blocks: eight first-stage 6-bit SAR sub-ADCs, an analog multiplexer, a multiplying digital-to-analog converter (MDAC), a second-stage 7-bit SAR sub-ADC and a synchronous output module. The first-stage 6-bit SAR ADC is in column parallel architecture. The ADC works

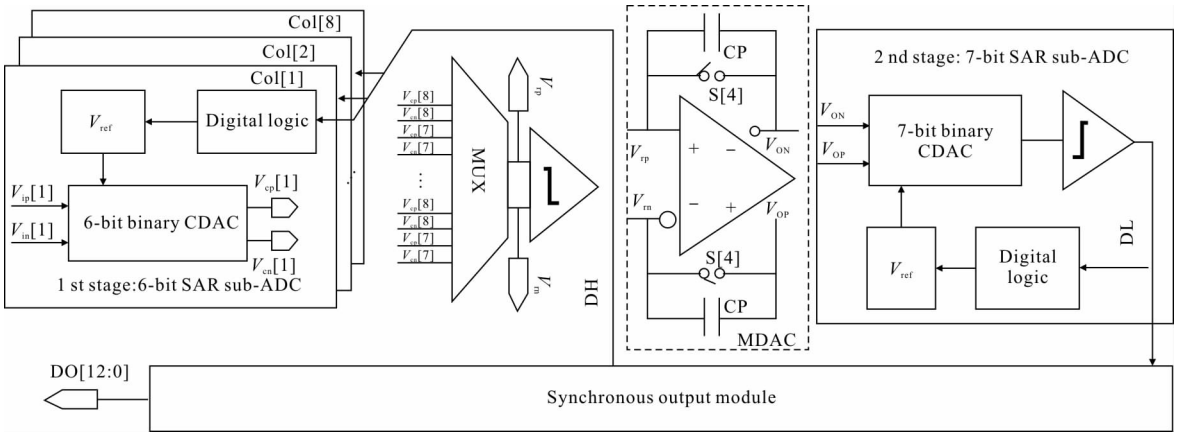

Fig.2 Proposed multiple-columns-shared-parallel pipeline-SAR ADC

as follows. Firstly, eight preprocessing analog pixel signals are sampled by the corresponding first-stage 6-bit sub-ADCs simultaneously. Secondly, the multiplexer strobes different column pixel signal into the comparator. Then, the first stage SAR sub-ADC converts the preprocessing pixel signal to 6-bit digital code, and produces a corresponding residual signal in sequence. After that, the MDAC amplifies the residual signal, which is sampled on the second stage SAR sub-ADC. Then, the second-stage SAR sub-ADC converts it to 7-bit digital code. Finally, the output register synchronizes the first-stage and second-stage output digital code. Digital error correction is performed off-chip. The ADC resolves 12-bit after digital error correction with a single bit of stage redundancy.

Compared to the full resolution SAR ADC, this multiple-columns-shared pipeline-SAR ADC reduces the conversion steps and the total capacitance of the CDAC, and relaxes the accuracy requirements on the sub-ADC. The pipeline-SAR ADC make full use of the SAR ADC′s simplicity and area advantage. Compared to the pipeline ADC, this multiple-columns-shared pipeline-SAR ADC reduces the stages and power consumption, but makes full use of the high speed and high resolution advantage. This proposed multiple-columns-shared pipeline-SAR ADC is shared by 8-column pixels, and can significantly relax physical design effort of the ADC. Consequently, this proposed pipeline-SAR ADC is suitable for the high speed high resolution CIS with small pixel pitch.

2 Circuit design

2.1 Architecture of the SAR sub-ADC

The sub-ADC′s circuits for the first-stage and second-stage are same, but the resolutions are different, one is 6-bit and the other is 7-bit. The architecture of the sub-ADC is shown in Fig.3. It consists of three main building blocks: a charge redistribution binary-weighted CDAC, a comparator and an asynchronous feedback logic block. After the first-stage finishes quantization, the residue signal is kept on the top plate of the CDAC array. This residue signal will be taken by MDAC for amplification.

The first stage SAR sub-ADC performs sampling the preprocessed pixel signal and conversion. The second stage SAR sub-ADC performs two operations: sampling the amplified residue and conversion. The SAR sub-ADC operates as the asynchronous timing diagram shown in Fig.4. When Samp1 is high, the bottom plates of the first stage CDAC capacitors are connected to the input difference pixel signal, and the top plates of the capacitors are connected to V_{cm}. Once Samp1 falling edge coming, the input difference pixel signal is sampled on the

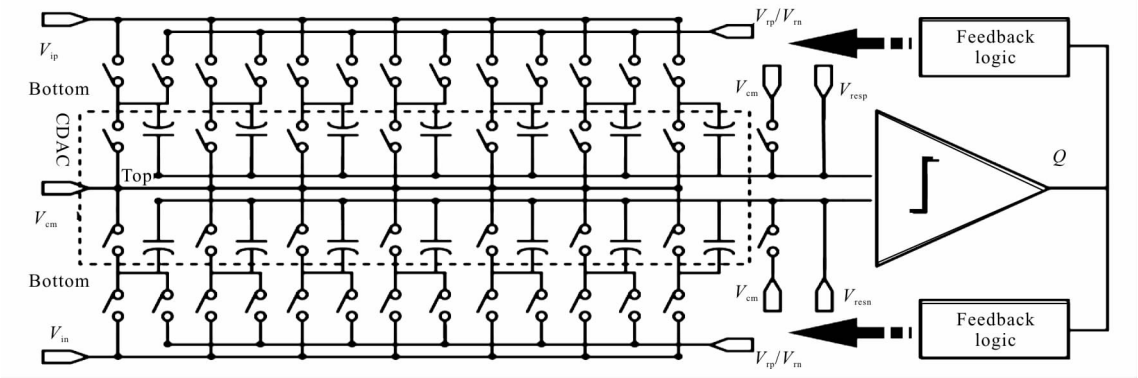

Fig.3 Circuit of the SAR sub-ADC

capacitive array and the asynchronous logic is triggered. Then, PH1 turns to high level and the bottom plates of the first stage CDAC capacitors are connected to V_{cm}. The asynchronous logic automatically generates the comparison signal COMP1 according to the comparator output. When the LSB comparison finishes, PHMDAC changes to high level which enables the MDAC to amplify the residue. After PHMDAC falls to low level, the comparison of the second stage SAR sub-ADC starts according to COMP2. At the same time, the first stage SAR sub-ADC starts for the next conversion.

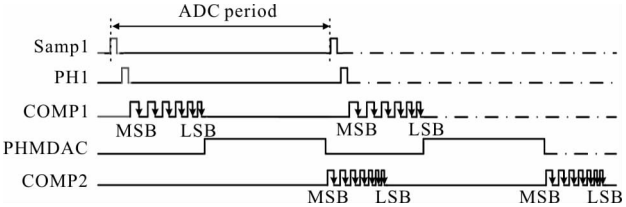

Fig.4 Asynchronous time diagram

The asynchronous logic is useful to improve the conversion speed of the CDAC. For an N-bit SAR ADC, it needs N conversion steps to complete the comparison. If synchronous logic is implemented in the SAR ADC, the conversion period T_{syn} is proportional to the maximum single conversion step time, and it is expressed as:

$$T_{syn}=N*K*\ln\left(\frac{V_{FS}}{V_{min}}\right) \tag{1}$$

If asynchronous logic is implemented, the conversion period T_{asy} for a sample is expressed as:

$$T_{asy}=\sum_{i=0}^{N-1}K*\ln\left(\frac{V_{FS}}{V_{res[i]}}\right) \tag{2}$$

where K is a constant coefficient decided by the comparator; V_{FS} is the full scale input voltage of the sub-ADC; V_{min} is the minimum input voltage of the comparator, $V_{res[i]}$ is the input voltage of the i-th comparison process. V_{min} can be less than the least significant bit (LSB) size difference voltage Δ. $V_{res[i]}$ is always larger than Δ, and can be quickly compared. In this design, the clock frequency is 50 MHz, and the first stage SAR sub-ADC needs 6-clock cycles to complete the comparison of one sample using synchronous logic. However, asynchronous logic can automatically adjust the compared time for each step according to the input voltage amplitude. Therefore, the sub-ADC completes the comparison of one sample within 1-clock cycle with asynchronous logic. For the same input clock frequency, asynchronous logic has a great speed advantage. Otherwise, synchronous logic consumes more power for same sampling rates, because it calls for much higher clock frequency.

2.2 Accuracy of the SAR sub-ADC

Thermal noise is the first important factor to affect the accuracy of the SAR ADC. For an N-bit full ADC resolution, the input equivalent noise power should be smaller than the quantization noise power [12]. The limited condition is presented as:

$$2*\frac{K*T}{C_t}<\frac{\Delta^2}{12} \tag{3}$$

where K is the Boltzmann constant, T is the Kelvin temperature, C_t is the total capacitance of the CDAC. There are three main noise sources for the proposed pipeline SAR ADC including the first stage CDAC capacitors, the MDAC and the second stage CDAC capacitors. In fact, the input referred noise power of the second stage CDAC is decreased by the gain amplification of the MDAC, which is useful for reducing the unit capacitor of the second stage CDAC. The total noise power is partitioned between the three main noise sources.

The mismatch of the capacitive array is another crucial restriction to the full ADC resolution. Generally, DNL and INL are the most useful statistical indicators to reflect the effect of mismatch. Assuming that the mismatch of a unit

capacitor C_u is σ_u, a nominal LSB capacitor C_i fits normal distribution, which is presented as:

$$C_i \sim N\left(C_i, \left(\sigma_u * \sqrt{\frac{C_u}{C_i}}\right)^2\right) \tag{4}$$

The worst case for the DNL and INL is presented as:

$$(DNL)_{max} \approx \sqrt{2^N} * \sigma_u \tag{5}$$

$$(INL)_{max} \approx \sqrt{2^N - 1} * \sigma_u \tag{6}$$

As can be seen, the worst DNL and INL are proportional to σ_u. σ_u depends on the capacitance area and process accuracy. Generally, the worst DNL and INL should be within +/−1 LSB. The minimum mismatch of the unit capacitor is obtained from the requirements on the DNL and INL. Appropriately size capacitors can achieve required mismatch percentages, which can be calculated according to the mismatch parameter in the process technical file provided by the foundry.

Finally, the capacitor size is determined by considering the thermal noise and the linearity requirements. Since the first stage CDAC has a large capacitance to achieve small KT/C noise power and to satisfy the linearity requirements of the full ADC resolution, the first stage unit capacitor is 32 fF and MIM capacitor is used as the unit capacitor. As a result, the first stage CDAC draws a considerable amount of power. With the implementation of a single bit redundancy and residue amplification, the second stage sub−ADC has a much more relaxing requirement on the CDAC and comparator. The accuracy of the second stage CDAC and comparator just need to satisfy the requirements of the sub−ADC resolution. Therefore, the second stage unit capacitor is 4 fF and the MOM capacitor is used as the unit capacitor.

The architecture of the comparator is the traditional dynamic comparator. It contains a dynamic preamplifier and a latch. The dynamic preamplifier is used to amplify the input differential signal and suppress the offset and noise of the dynamic latch. The comparator of the first stage is shared by the eight sub−ADCs as shown in Fig.2, which is helpful to decrease the area of the ADC. The accuracy of the comparator is also critical for high resolution SAR sub−ADC. The noise of the comparator affects the comparison result of the small input signal. It depends on the effective integration time, overdrive voltage and output load capacitance of the dynamic preamplifier. The comparator must be able to quantify 1 LSB input difference signal. Different from the full resolution SAR ADC, the noise of the comparator should be smaller than the LSB size difference voltage of the first stage sub−ADC and second stage sub−ADC, respectively. In consideration of the 1−bit redundancy, the offset of comparator is must be lower than 1 LSB, otherwise the output of the MDAC will exceed the full scale voltage of the second stage sub−ADC.

2.3 MDAC

MDAC is a core block for the pipeline SAR ADC. Figure 5 (a) shows the architecture of the MDAC. It mainly consists of an opamp and switched−capacitors. Timing diagram is shown in Fig.5 (b). It performs three operations: subtraction, multiplication, sampling and holding function. The residue is gotten by subtracting the DAC output from the input analog signal. The residual signal is zoomed in an appropriate ratio so that each stage has the same reference voltage. In order to avoid the overloading of the second stage sub−ADC, the MDAC is implemented with 1 −bit redundancy. 1 −bit redundancy provides additional offset headroom to relax the requirements on the comparator offset. In addition, MDAC is also used to sample and hold the residual signal for the second stage sub−ADC. The amplified residue is expressed as:

$$V_{\mathrm{op}}-V_{\mathrm{on}}=-\frac{C_s}{C_f}*(V_{\mathrm{rn}}-V_{\mathrm{rp}})*\frac{\beta*A_0}{1+\beta*A_0}*\left(1-e^{\frac{-t}{\tau}}\right) \quad (7)$$

Where C_s is the total capacitance of the CDAC, C_f is the feedback capacitor of the MDAC, here is $4C_{\mathrm{u}}$, $V_{\mathrm{rn}}-V_{\mathrm{rp}}$ is the residue of the first stage SAR sub-ADC, β is the feedback factor of the MDAC, A_0 is the open loop gain of the opamp, $\tau=1/(\beta A_0\omega_0)$ is the settling time constant of the MDAC.

The precision of the residue determines the resolution of the overall ADC. The settling time of the MDAC limits the conversion speed of the ADC. The error of the MDAC contains static error and dynamic error. The static error and dynamic error are presented as:

$$\varepsilon_s\frac{1}{(\beta*A_0)}\leqslant\frac{\Delta_2}{2} \quad (8)$$

$$\varepsilon_D=\mathrm{e}^{\frac{-t}{\tau}}\ll\frac{\Delta_2}{2} \quad (9)$$

Δ_2 is LSB size difference voltage of the second stage sub-ADC. By solving the above two equations, A_0 should be more than 73 dB, and the loop gain should be greater than 25 MHz.

In general MDAC designs with 1-bit redundancy, the closed loop gain of the MDAC is 2^{N-1}, which leads to a small feedback factor and small closed loop bandwidth. As a result, it places a strict requirement on the GBW of the opamp. The opamp is hence power hungry. A half-gain MDAC architecture is used to alleviate this problem. In half-gain MDAC architecture, the closed loop gain is reduced to 2^{N-2}, the feedback factor is increased by about 2. The half-gain MDAC architecture is effective to reduce the

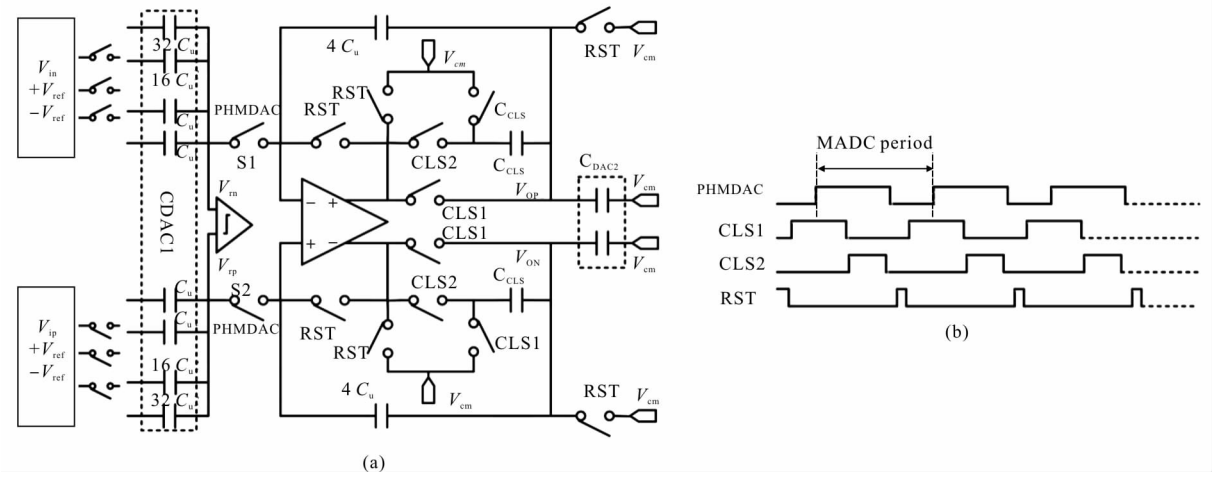

Fig.5 (a) Architecture of the MDAC, (b) time diagram of the MDAC

GBW and power consumption of the opamp. One disadvantage is that the usage of a half-gain MDAC reduces the MDAC output swing from $V_{\mathrm{ref/2}}$ to $V_{\mathrm{ref/4}}$. To obtain the same resolution as the full gain MDAC architecture, the reference voltage of the second stage SAR sub-ADC is also reduced to $V_{\mathrm{ref/2}}$. The requirements for a 7-bit second stage SAR sub-ADC in half-gain MDAC design is actually like an 8-bit SAR sub-ADC in full-gain MDAC design.

Additionally, in order to reduce the static error due to the finite loop gain, correlated level shift technique[13] is utilized in the MDAC. Level shift technique is a switch capacitor technique that is helpful to improve the equivalent open loop gain. As shown in Fig.6(a) and Fig.6(b), switches controlled by CLS1 and CLS2 make up the level shift network, level shift technique operates in two steps: the first step is estimation, CLS1 and PHMDAC changes to high level successively,

MDAC output the estimated amplified voltage on capacitor C_{CLS} and C_{DAC2}. The estimated static settling output V_e can be expressed as:

$$V_e=-\frac{C_s}{C_f}*(V_{rn}-V_{rp})*\frac{T_0}{1+T_0} \tag{10}$$

where T_0 is the loop gain. Secondly, CLS1 changes to low level and CLS2 changes to high level, charge stored in capacitor C_{CLS} transfers to capacitor C_{DAC2}, MDAC completes precise amplification. The final precise amplifying static settling output voltage is presented as:

$$V_o=-\frac{C_s}{C_f}*(V_{rn}-V_{rp})*\frac{T_e}{1+T_e} \tag{11}$$

$$T_e\approx\frac{T_0^2}{\lambda+1} \tag{12}$$

$$\lambda=\frac{C_S*C_f}{C_{CLS}*(C_S+C_f)}+\frac{C_{DAC2}}{C_{CLS}} \tag{13}$$

where T_e is the equivalent loop gain using level shift technique, λ is a coefficient depends on the capacitor C_{CLS}. As can be seen, for given C_s, C_f and C_{DAC2}, λ is inversely proportional to capacitor, but T_e is proportional to C_{CLS} and T_0^2. Therefore, the static error with level shift technique decreases effectively as $1/T_e$, which immensely reduce the requirement on the open loop gain of the opamp. The MDAC open loop gain A_0 could be less than 60 dB. A cascade amplifier is used as the opamp of the MDAC. By using the level shift technique, the cascade amplifier can easily get a very large equivalent open loop gain just with very small cost of two capacitor C_{CLS} and several switches. Compared with the MDAC using complicated gain-boost amplifier in reference [6], the design of this MDAC is easier and the area is much smaller.

2.4 Digital error correction

The digital error correction is performed off-chip. The ADC resolves 12-bit after digital error correction with a single bit of stage redundancy. The full ADC decimal output is expressed as:

$$D_{out}=K_r*[D_{12},D_{11},\cdots,D_7]*[W_{12},W_{11},\cdots,W_7]^T+[D_6,D_5,\cdots,D_0]*[W_6,W_5,\cdots,W_0]^T \tag{14}$$

where K_r is the amplifying coefficient for the first stage output digital code, $[D_{12},D_{11},\cdots,D_7]$ and $[D_6,D_5,\cdots,D_0]$ are the binary output code of the first stage and second stage SAR sub-ADC, respectively. $[W_{12},W_{11},\cdots,W_7]$ and $[W_6,W_5,\cdots,W_0]$ are the weight coefficient of the first stage and second binary CDAC. The off-chip digital error correction can calibrate the MDAC gain error by adjusting K_r, and can also calibrate the mismatch of the CDAC by adjusting weight matrix $[W_{12},W_{11},\cdots,W_7]$ and $[W_6,W_5,\cdots,W_0]$.

3 Simulated results

This work is fabricated in a 0.18 μm 1P4M CMOS image sensor process. A 260×130 pixel array of 7.5 μm pitch 4*T* pixel and the proposed circuits are implemented on a 3.8 mm×4.9 mm die. This multiple-columns-shared-parallel pipeline SAR ADC occupies 0.204 mm^2 for 8 columns. The layout is shown in Fig.6 (a). The resolution is 12-bit divided by 6-bit coarse and 7-bit fine SAR sub-ADC with 1-bit redundancy calibration between coarse and fine steps. The input full scale voltage is 1 V. The simulated spectrum is as shown in Fig.6(b). The ADC achieves a simulated SNDR of 72.6 dB with a 229.7 kHz input and 71.7 dB with 4.16 MHz input at 8.33 Msps. It dissipates 4.95 mW at 1.8 V supply and the figure of merit (FoM) is 172.5 fJ/conversion-step. Table 1 shows the performance of ADC and compares the performance with other ADCs for high-speed CIS. This proposed pipeline-SAR ADC is very suitable for the high speed CIS based on its better area, FoM performance and higher resolution.

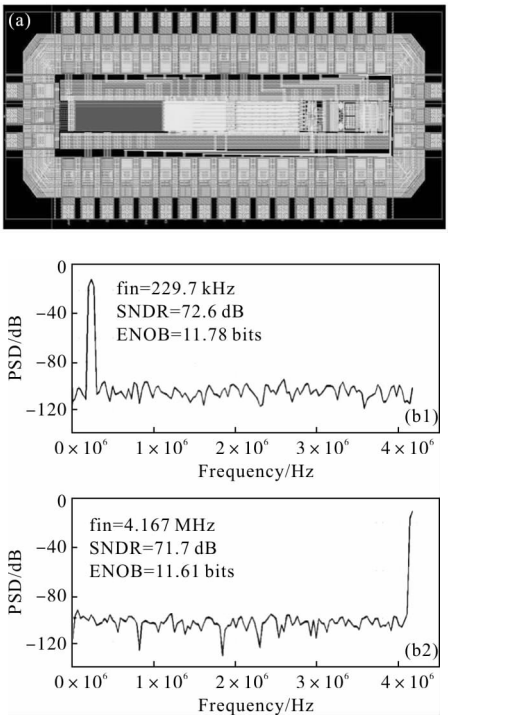

Fig.6 (a) Layout of the proposed pipeline SAR ADC; (b) Simulated spectrum

Tab.1 Performance comparisons with other ADC for high-speed CIS

	Ref.[8]	Ref.[10]	This work
Type	Cyclic	SAR	Pipeline SAR
Process	0.13 μm 1P3M	0.18 μm 1P6M	0.18 μm 1P4M
Supply voltage/V	3.3	1.8	1.8
Resolution/bit	10	10	12
Sample rate	1.6 Msps	240 Ksps	8.33 Msps
ENOB/bit	7.83	8.22	11.76
Power/mW	0.736	35.46	4.95
FOM/fJ·step	2000	495.5	172.5
Area/mm^2	0.019 6	0.109	0.204

4 Conclusion

A 12-bit multiple-columns-shared-parallel pipeline SAR ADC for high speed CIS is proposed. A 260×130 pixel array of 7.5 μm pitch 4*T* pixel and the proposed circuits are implemented on a 3.8 mm×4.9 mm die. The ADC is implemented within 16 pixel pitches and designed in 0.18 μm 1P4M CIS process. Digital error correction is performed off-chip. The ADC resolves 12-bit after digital error correction with a single bit of stage redundancy. The simulated ENOB of the SAR ADC is 11.76 bit, which has a higher resolution than the works in Ref. [8] and [10]. The sample rate is 8.33 Msps, which is faster than the works in Ref. [8] and [10]. It dissipates 4.95 mW at 1.8V supply and the FoM is 172.5 fJ/conversion-step, which consumes less power than the works in Ref. [8] and [10]. This multiple-columns-shared-parallel pipeline SAR ADC occupies 0.204 mm^2 for 8 columns, only 0.0255 mm^2 for one column, which is more compact than the SAR ADC in Ref. [10]. Though the area is larger than that in Ref. [8], the other performances are better. With higher resolution, better FoM performance an smaller area, this proposed pipeline SAR ADC is suitable for the high speed CIS.

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