

Monolithic integration of a wavelength division multiplexer/ demultiplexer and electro-absorption VOAs based on 3 μm -SOI

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Abstract: Wavelength division multiplexers/demultiplexers and variable optical attenuators(VOAs) are key devices used in optical communication systems. In order to get their monolithic integrated chip with simple fabrication process and fast time response, and considering the possibility of it to integrate with other different optical devices, a 16-channel 200 GHz arrayed waveguide grating (AWG) multiplexer/demultiplexer was monolithically integrated with electro-absorption variable optical attenuators on a silicon-on-insulator (SOI) platform. The on-chip loss was less than 7 dB and the crosstalk was less than -22 dB. The power consumption of the electro-absorption VOA is 572.4 mW (106 mA, 5.4 V) at 20 dB attenuation. Besides, the device provides fast optical power attenuation, and in a 0-5 V square voltage, the rising/falling time of the VOA is 50.5 ns and 48 ns, respectively.

Key words: arrayed waveguide grating; variable optical attenuator; silicon photonics; silicon on insulator

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基于 3 μm -SOI 的波分复用/解复用器与电吸收型 VOA 的单片集成

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摘 要: 波分复用/解复用器与可调光衰减器的是光通信系统中的重要元器件。为了得到制备工艺简单、响应速度快的二者的单片集成芯片, 并且考虑到其与其他不同光器件的集成可能性, 在绝缘体上硅材料制作了 16 通道、信道间隔 200 GHz 的阵列波导光栅复用/解复用器与电吸收型可调光衰减器的单片集成。该器件的片上损耗小于 7 dB, 串扰小于 -22 dB。电吸收型 VOA 在 20 dB 的衰减量下的功耗为 572 mW(106 mA, 5.4 V)。此外, 该器件可以实现光功率的快速衰减, 在 0~5 V 的外加方波电压下, VOA 上升及下降时间分别为 50.5 ns 和 48 ns。

关键词: 阵列波导光栅; 可调光衰减器; 硅基光子学; 绝缘体上硅

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0 Introduction

With the rapid development of the global internet, the demand for communication capacity and transmission rate is increasing dramatically, which can be solved by Wavelength Division Multiplexing (WDM) technology because of its ability to expand the bandwidth of optical communication network. Arrayed Waveguide Gratings (AWGs)^[1-4] and Variable Optical Attenuators (VOAs)^[5-7] are very important passive optical waveguide devices in WDM systems. AWGs with wavelength-division multiplexing/demultiplexing function can realize different optical signal transmission in one fiber or one waveguide, and can take advantage of the huge bandwidth of the fiber to realize the network capacity expansion of the optical communication system. Variable optical attenuators can balance the optical power of signals in each channel and consequently realize the error-free and long-distance optical signal transmission. Thus it is expected that the integration of AWG and VOA can achieve optical wavelength multiplexing/demultiplexing and optical power equalizing, and enhance the reliability and reduce the cost of the WDM system.

Previously, some monolithic integration structures of AWG and VOA have been reported, such as an AWG with thermo-optic VOAs fabricated on SOI with 2 μm top silicon layer which has a relatively slow time response^[8], a monolithic heterogeneous integration of a silica-based AWG with a SOI-based electro-absorption type VOA array which must take sophisticated fabrication process^[9], and an integrated chip of an AWG with thermo-optic VOAs based on silica, which can't realize the monolithic integration with other functional devices^[10]. So it can be concluded that AWGs integrated with electro-absorption type VOAs based on SOI is more preferable, which exhibits fast response speed, takes simple manufacturing technique, and can monolithically integrated with other optical devices. Recently, AWGs and VOAs based on

SOI with submicron top silicon layer have been attracting attention and are recognized as the most promising solution for optical communication system in the future because they have small footprint and high integration rate. However, the performance of AWGs and VOAs based on submicron SOI is sensitive to the waveguide dimensions which leads to the requirement for higher fabrication precision and poorer performance than ideal. On the other hand, AWGs and VOAs based on submicron SOI must take e-beam lithography or ultraviolet lithography, which is to the disadvantage of realizing the mass production.

In this paper, we have demonstrated an integration chip of an AWG with an electro-optical VOA array on SOI platform with 3 μm top silicon layer, which can be fabricated by photolithography. The photolithography is a mature semiconductor process, which is more cost-effective, and waveguides based on micron SOI require relatively lower lithography precision and thus having higher overall yields.

1 Design and fabrication

Figure 1 (a) is the structural diagram of the device, which consists of a 3×16 AWG with channel spacing of 200 GHz and a 16-channel electro-absorption (EA) type VOA array. The AWG is composed of input/output waveguides, arrayed waveguides and input/output free propagation regions (FPRs). The EA-type VOA is designed according to the plasma dispersion effect of silicon, which is composed of a rib waveguide and 4 lateral p-i-n diodes connected in series, as shown in Fig.1. Inset1 in Fig.1 is the structure of the ridge waveguide, inset2 is the tapers between the input/output/arrayed waveguides and the FPRs, inset3 is the top view of the EA-type VOA, and inset4 is the cross-sectional structure of the EA-type VOA.

The AWG and EA-type VOA integrated device

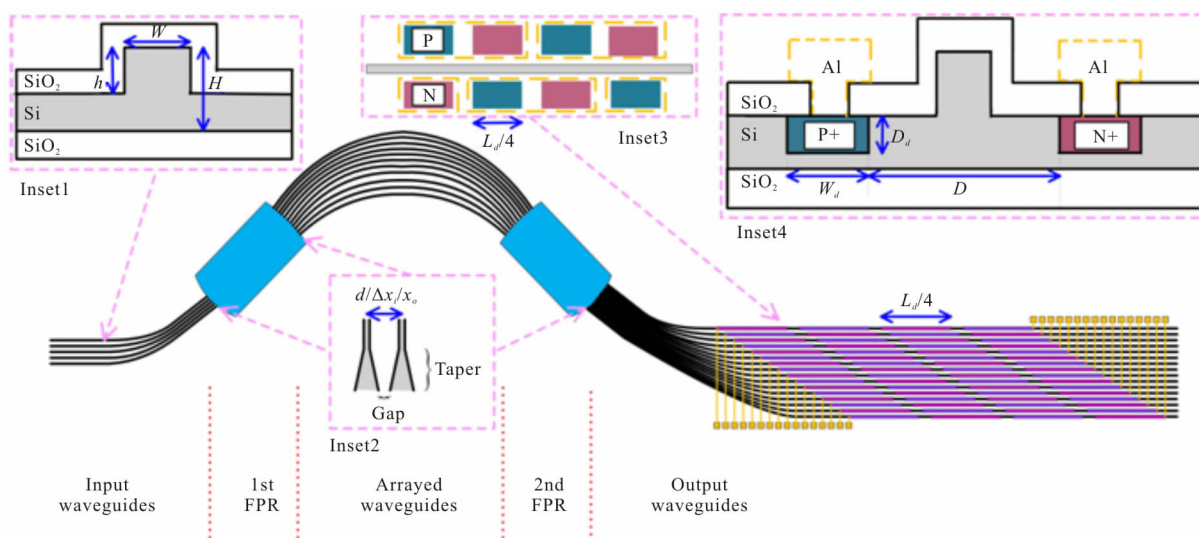


Fig.1 Structural diagram of the monolithic integration of an AWG with an EA-type VOA array based on a 3 μm-SOI platform

is fabricated on SOI wafer with 3 μm top silicon layer (H), and ridge waveguides are used to ensure the single mode propagation. The width (W) and etching depth (h) of the waveguides are 3 μm and 1.2 μm respectively. The optical field distributions of TE₀ mode and TM₀ mode are shown in Figs.2(a) and (b), respectively.

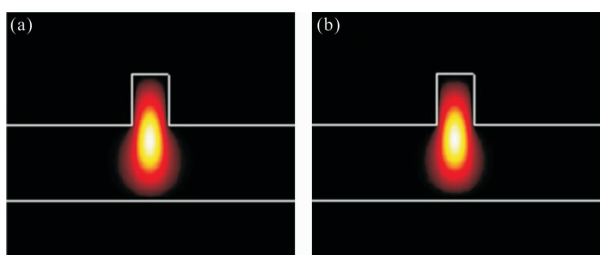


Fig.2 Optical field distributions of TE₀ mode (a) and TM₀ mode (b)

In AWG devices, a lot of bent waveguides are used to get a compact structure and thus decreasing the footprint of the AWGs. Bent waveguides will introduce bending loss and smaller bent radius results in smaller device size but larger bending loss, so the normalized output optical power of a bent waveguide with different bent radius is simulated, as shown in Fig.3. With the radius of the bent waveguide growing larger, the normalized output optical power rises at the beginning and then tends to keep stable when the bent

radius is larger than 3 200 μm. So it's obvious that the minimum radius of bent waveguides in AWG must be larger than 3 200 μm. In this paper, we set the minimum bent radius to be 3 500 μm.

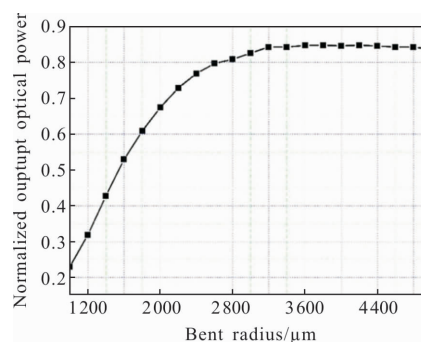


Fig.3 Dependence of the normalized optical power on the bent radius of the bending ridge waveguide

The minimum distance between input waveguides (Δx_i), output waveguides (Δx_o) and arrayed waveguides (d) are very important parameters in AWG. Small values of them will lead to the mutual coupling between two waveguides and then will cause extra crosstalk, but too large value of them will increase the overall footprint of AWG. The mutual coupling between two straight waveguides is simulated using beam propagation method (BPM), as shown in Fig.4. Figures 4(a) and (b) show the optical field distribution

and the monitored launch power of both waveguides (Wg.1 and Wg.2) along Z direction when the distance between the two straight waveguides (D) is $6\ \mu\text{m}$ and $9\ \mu\text{m}$. The optical signal in Wg.1 is easily coupled into Wg.2 when their distance is $6\ \mu\text{m}$, so the launch power in Wg.1 (1 launch) decreases and the launch power in Wg.2 (2 launch) increases along Z direction. But when the distance between Wg.1 and Wg.2 is $9\ \mu\text{m}$, there is hardly any coupling between them.

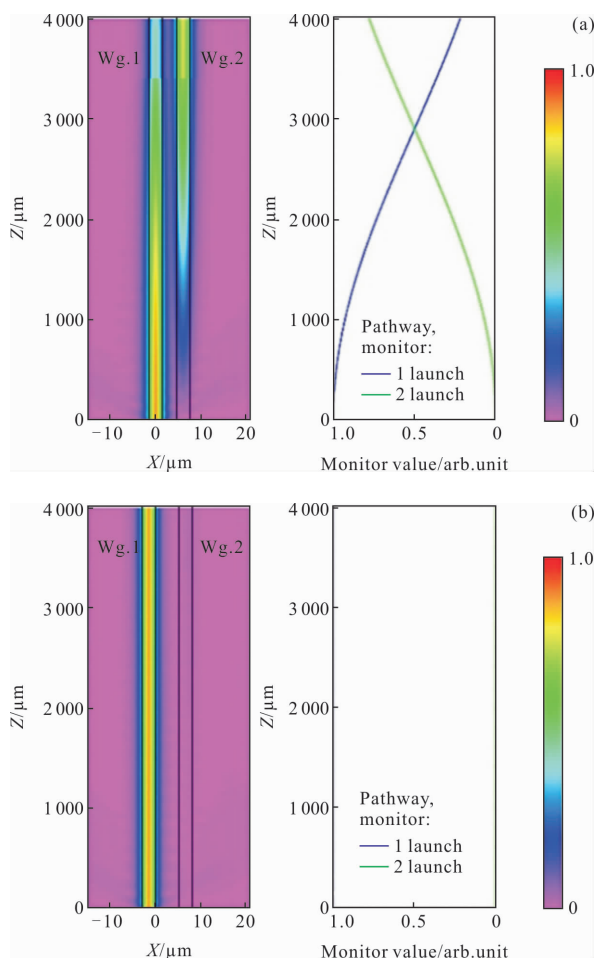


Fig.4 Optical field distribution and monitored launch power of two straight waveguides with distance of $6\ \mu\text{m}$ (a) and $9\ \mu\text{m}$ (b)

The normalized output optical power of the two straight waveguides under different distance between them is simulated, as shown in Fig.5. From Fig.5 we can see that as the distance of two straight waveguides grows small, the mutual coupling between them is increasingly evident, and when the distance between the two straight waveguides is larger than $9\ \mu\text{m}$,

the coupling between them can be neglected. In this paper, the value of the minimum distance between adjacent arrayed waveguides (d) is $9\ \mu\text{m}$, and the value of the minimum distance between adjacent input/output waveguides ($\Delta x_i/\Delta x_o$) is $10\ \mu\text{m}$.

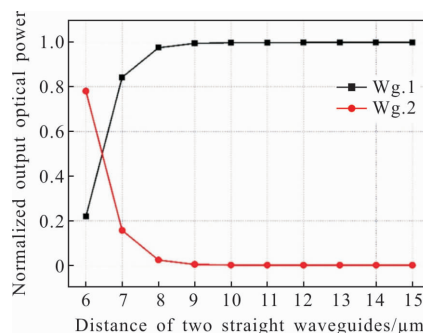


Fig.5 Dependence of the normalized output optical power on the distance between two straight waveguides

Another important design in AWG is the taper located at the joint of FPRs and input/output/arrayed waveguides. Tapers are usually used to connect the FPRs and the input/output/arrayed waveguides to decrease the mode mismatching between them. These tapers are expected to be wide enough, which can reach to the minimum distance between the adjacent input/output/arrayed waveguides ($\Delta x_i/\Delta x_o/d$) theoretically to receive as much light as possible, but considering the fabrication limitation, there always leaves a narrow gap (usually $1\ \mu\text{m}$) between two adjacent tapers. On the other hand, the tapers also should be long enough for low-loss mode conversion. However, the narrow gaps and long coupling distances between adjacent tapers may also cause the degradation of crosstalk in AWG. So it is expected to select a relatively short taper length, which must simultaneously realize the smooth mode conversion to decrease the insertion loss and small optical coupling distance to decrease the crosstalk. Figure 6 is the simulated dependence of normalized output optical power on the length of taper, from which we can conclude that when the taper length is larger than $100\ \mu\text{m}$, the low-loss mode conversion from the FPR to the input/output/arrayed waveguides can be achieved. Finally, the length of the

taper is designed to be 150 μm .

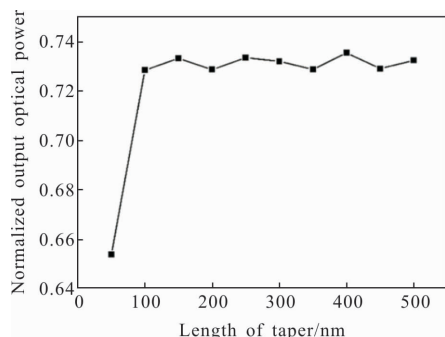


Fig.6 Dependence of the normalized output optical power of taper on its length

The detailed design parameters are listed in Tab.1.

Tab.1 Designed parameters of the monolithic integration of an AWG and an EA-type VOA array

Parameter	Symbol	Value
Thickness of top silicon layer	$H/\mu\text{m}$	3
Width of ridge waveguides	$W/\mu\text{m}$	3
Thickness of outer-ridge slab waveguides	$h/\mu\text{m}$	1.8
Doping distance	$D/\mu\text{m}$	10
Doping width	$W_d/\mu\text{m}$	10
Doping depth	$D_d/\mu\text{m}$	0.9
Doping length	L_d/cm	1
Doping concentration	C_d/cm^{-3}	1×10^{19}
Structure	-	Series
The minimum distance between input/output waveguides	$(\Delta x_i/\Delta x_o)/\mu\text{m}$	10
Channel spacing	$\Delta\lambda/\text{nm}$	1.6
Number of input/output waveguides	N_i/N_o	3/16
The minimum distance between arrayed waveguides	$d/\mu\text{m}$	9
Central wavelength	$\lambda_0/\mu\text{m}$	1.55

The micrographs of the fabricated monolithic integration of AWG and VOA array are shown in Fig.7. Figure 7(a) is the overall structure, (b) is the structure of input waveguides, (c) is structure of the arrayed waveguides, (d) is the structure of output waveguides and (e) is the via electrodes and doping areas.

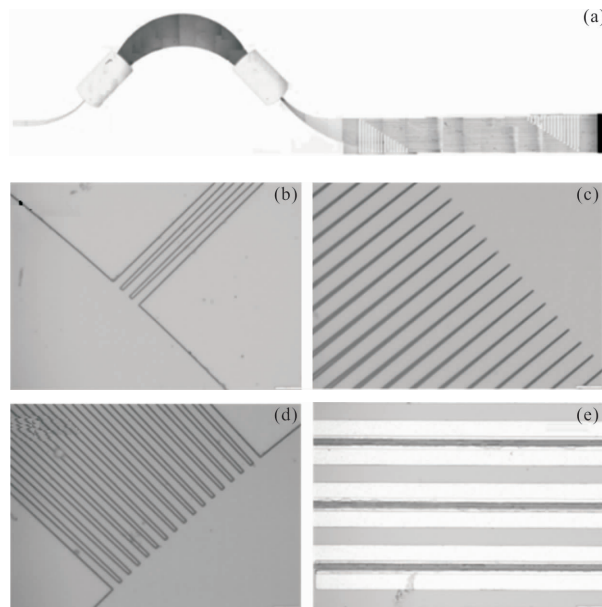


Fig.7 Micrographs of the monolithic integration of AWG and EA-type VOAs

2 Measurement and discussion

The testing system of the monolithic integration of AWG and EA-type VOAs is shown in Fig.8. The integrated chip is placed in the 6-axis adjustment

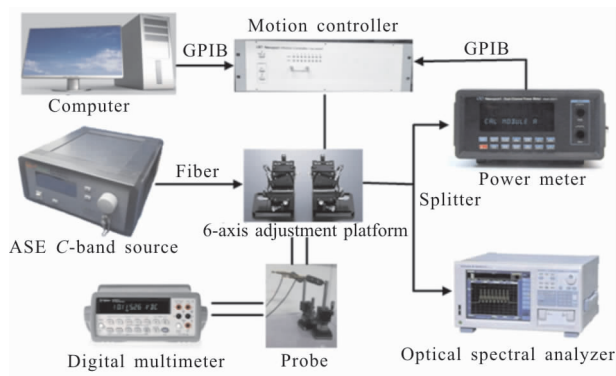


Fig.8 Testing system of the monolithic integration of AWG and EA-type VOAs

platform. The optical signal from a C-band ASE (Amplified spontaneous emission) source is coupled into a input waveguide of the integrated chip by a single-mode lens fiber. The output waveguides of the integrated chip are connected to a power meter and an optical spectral analyzer through a splitter. Motion controller is used to realize the precise control of the

6-axis adjustment platform. Different DC voltage values from the digital multi-meter are applied to the VOA electrodes of the integrated chip through two probes.

First the spectrum of the integrated chip without applying voltage to the VOA part is tested, as shown in Fig.9. The maximum on-chip loss of the 16-channel AWG is about 7 dB and the maximum crosstalk is about -22 dB. The central wavelength is 1 550.48 nm, shifting 0.48 nm from the designed wavelength. The wavelength shift is partially caused by the difference between the measurement temperature and the designed temperature of AWG, and partially caused by the waveguide dimension deviation from the designed value in the fabrication process.

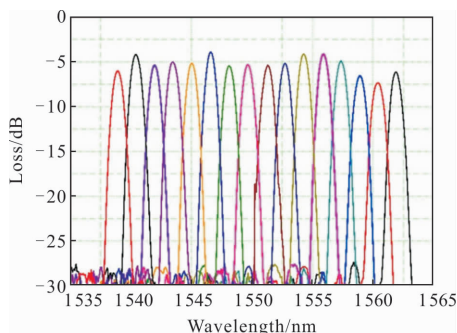


Fig.9 Demultiplexing with 200 GHz spacing in fabricated device

Then the performance of the VOA part of the integrated chip is tested, as shown in Fig.10. Figure 10(a) is the relationship between the attenuation and the injected current, (b) is the dependence of injected current on the applied voltage, and (c) is the dependence of the attenuation on the power consumption. The attenuation and injected current of the VOA are basically linear fitted, and the power consumption of the VOA is 572.4 mW (106 mA, 5.4 V) at 20 dB attenuation.

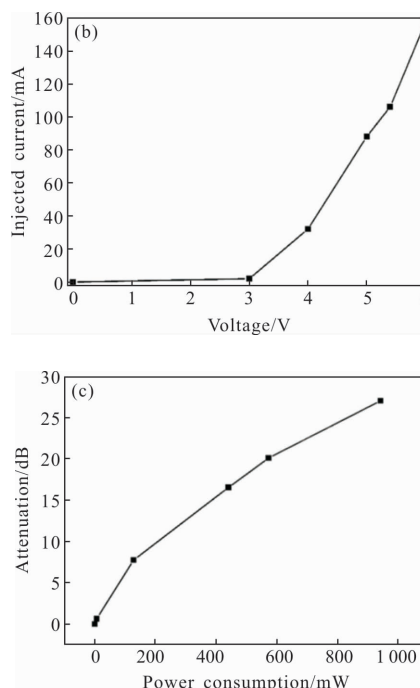
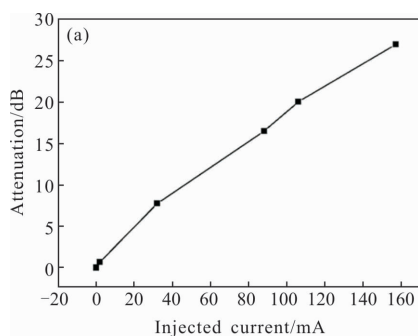
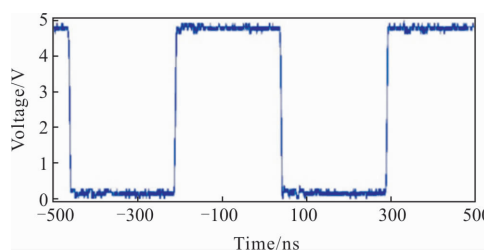


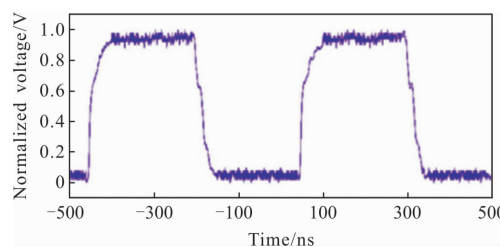
Fig.10 Performance VOA part of the integrated chip

The time response of the VOA part in the integrated chip is tested, as shown in Fig.11. With high/low level of the applied square voltage being 0 V/5 V, the rising/falling time of the VOA is 50.5 ns/48 ns, respectively.

Finally, the normalized output spectrum of the integrated chip is tested with different voltage values



(a) A square voltage with high/low level of 0 V/5 V applied to the Si VOA



(b) Measured dynamic response curve of the VOA

Fig.11 Time response of the Si VOA

being applied to the 16 VOAs to get different level of attenuation, as shown in Fig.12. 0/5/10/15/20 dB attenuation is achieved in channel 1–4/5–7/8–10/11–13/14–16, respectively. It can be concluded that the AWG–VOA integrated chip in this paper can realize excellent performance in wavelength de–multiplexing and fast optical power equalization in all 16 channels.

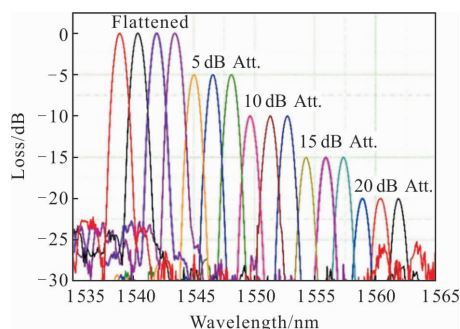


Fig.12 Tested normalized output spectrum of the integrated chip with different voltage values being applied to the 16 VOAs

3 Conclusions

In this paper, a monolithic integration of a 16–channel 200 GHz AWG multiplexer/demultiplexer and a 16–channel EA–type VOA array is designed and fabricated on SOI with 3 μm top silicon layer. The fabricated device shows an on chip loss of less than 7 dB and a crosstalk of less than –22 dB. The power consumption of the VOA part is 572.4 mW (106 mA, 5.4 V) at 20 dB attenuation and the rising/falling time of the VOA is 50.5 ns/48 ns, respectively. The integrated chip in this paper is expected to be applied to the large-capacity and high-speed optical communication system.

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